TECHNICAL MANUAL

ORGANIZATIONAL MAINTENANCE MANUAL
MAGNETIC TAPE UNIT

EXPANDED TROUBLESHOOTING
(LOGIC DIAGRAM THEORY)

GUIDED MISSILE
AIR DEFENSE SYSTEM
AN/TSQ-73

DEPARTMENT OF THE ARMY **5 JUNE 1984**

WARNING

DANGEROUS VOLTAGE

is used in the operation of this equipment

DEATH ON CONTACT

may result if personnel fail to observe safety precautions

Never work on electronic equipment unless there is another person nearby who is familiar with the operation and hazards of the equipment and who is competent in administering first aid. When the technician is aided by operators, he must warn them about dangerous areas.

Whenever possible, the power supply to the equipment must be shut off before beginning work on the equipment. Take particular care to ground every capacitor likely to hold a dangerous potential. When working inside the equipment, after the power has been turned off, always ground every part before touching it.

Be careful not to contact high-voltage connections when installing or operating this equipment.

Whenever the nature of the operation permits, keep one hand away from the equipment to reduce the hazard of current flowing through vital organs of the body.

WARNING

Do not be misled by the term "low voltage." Potentials as low as 50 volts may cause death under adverse conditions.

EXTREMELY DANGEROUS POTENTIALS
greater than 500 volts exist in the following units:
Display console high voltage power supply
Display console CRT

WARNING

For emergencies requiring immediate shutdown of system power, press SYSTEM POWER OFF switch located on power cabinet power transfer unit. Observe that SYSTEM POWER ON indicator light goes off.

LIST OF EFFECTIVE PAGES

Insert latest changes page, dispose of superseded pages in accordance with applicable regulations.

NOTE:

On a changed page, the portion of the text affected by the latest change is indicated by a vertical line in the margin of the page.

Dates of issue for original and change pages are:

Original .....0..... 5 Jun 84

Page No.	*Change No.	Page No.	*Change No.	Page No.	*Change No.
a	0	5-122 blank	0	5-177	0
b blank	0	5-123 - 5-126	0	5-178 blank	0
A	0	5-127	0	5-179 - 5-182	0
B blank	0	5-128 blank	0	5-183	0
i - v	0	5-129 - 5-130	0	5-184 blank	0
vi blank	0	5-131	0	5-185	0
5-1 - 5-84	0	5-132 blank	0	5-186 blank	0
5-85	0	5-133	0	5-187	0
5-86 blank	0	5-134 blank	0	5-188 blank	0
5-87	0	5-135 - 5-146	0	5-189	0
5-88 blank	0	5-147	0	5-190 blank	0
5-89 - 5-94	0	5-148 blank	0	5-191	0
5-95	0	5-149	0	5-192 blank	0
5-96 blank	0	5-150 blank	0	5-193 - 5-198	0
5-97	0	5-151 - 5-152	0	5-199	0
5-98 blank	0	5-153	0	5-200 blank	0
5-99	0	5-154 blank	0	5-201 - 5-202	0
5-100 blank	0	5-155	0	5-203	0
5-101 - 5-102	0	5-156 blank	0	5-204 blank	0
5-103	0	5-157 - 5-158	0	5-205	0
5-104 blank	0	5-159	0	5-206 blank	0
5-105	0	5-160 blank	0	5-207 - 5-208	0
5-106 blank	0	5-161	0	5-209	0
5-107 - 5-108	0	5-162 blank	0	5-210 blank	0
5-109	0	5-163 -5-164	0	5-211 - 5-212	0
5-110 blank	0	5-165	0	5-213	0
5-111	0	5-166 blank	0	5-214 blank	0
5-112 blank	0	5-167	0	5-215 - 5-216	0
5-113	0	5-168 blank	0	5-217	0
5-114 blank	0	5-169 - 5-170	0	5-218 blank	0
5-115 - 5-116	0	5-171	0	5-219	0
5-117	0	5-172 blank	0	5-220 blank	0
5-118 blank	0	5-173	0	5-221 - 5-222	0
5-119	0	5-174 blank	0	5-223	0
5-120 blank	0	5-175 - 5-176	0	5-224 blank	0
5-121	0				

*Zero in this column indicates an original page.

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No. 9-1430-655-20-5-2)

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, D.C., 5 June 1984

ORGANIZATIONAL MAINTENANCE MANUAL: MAGNETIC TAPE UNIT EXPANDED TROUBLESHOOTING (LOGIC DIAGRAM THEORY) GUIDED MISSILE AIR DEFENSE SYSTEM AN/TSQ-73

REPORTING OF ERRORS

You can help improve this publication. If you find any mistakes, or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in back of this manual direct to: Commander, U.S. Army Missile Command, ATTN: DRSMI-SNPM, Redstone Arsenal, AL 35898. A reply will be furnished to you.

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CHAPTER 5

MAGNETIC TAPE UNIT EXPANDED TROUBLESHOOTING

Section I. INTRODUCTION

5-1. Scope. The expanded troubleshooting part of TM 9-1430-655-20-5 of the Recorder-Reproducer RD-449/TSQ-73(V), hereinafter referred to as the magnetic tape unit (MTU), Equipment Maintenance for Guided Missile Air Defense System AN/ TSQ-73 is contained in volumes 2 and 3. It provides supplemental information for the use and guidance of advanced personnel responsible for repair of the MTU beyond the scope of organizational maintenance covered in the basic TM 9-1430-655-20 series of technical manuals.

5-2. Expanded Troubleshooting Concept. Expanded troubleshooting is required when existing fault isolation procedures in the basic manuals fail to isolate and correct a malfunction. The troubleshooting covered in this manual is based on the use of existing onsite equipment (tapes, tools, test equipment, spare parts, and publications). Isolation of malfunctions is based on the fault analysis of normal system operating conditions and the use of built-in maintenance and diagnostic (M&D) software programs.

5-3. Troubleshooting Aids. Volume 2 contains the detailed descriptions and the related functional block diagrams. The functional block diagrams are related to the functional logic diagrams in volume 3 by the titles of the functional areas. Power distribution diagrams, cabling diagrams, and front-panel schematic diagrams are also supplied in volume 3.

a. Input/Output Tables. Input and output tables are provided, as applicable, for each figure and sheet to enable easy access to signals referenced to other diagrams.

b. Input/Output Symbols. Symbols used on diagrams to indicate input and output signals include the following: *

▲ Indicates input from another figure.

△ Indicates input from the same figure.

■ Indicates output to another figure.

□ Indicates output to the same figure.

◪ Indicates output to the same and another figure.

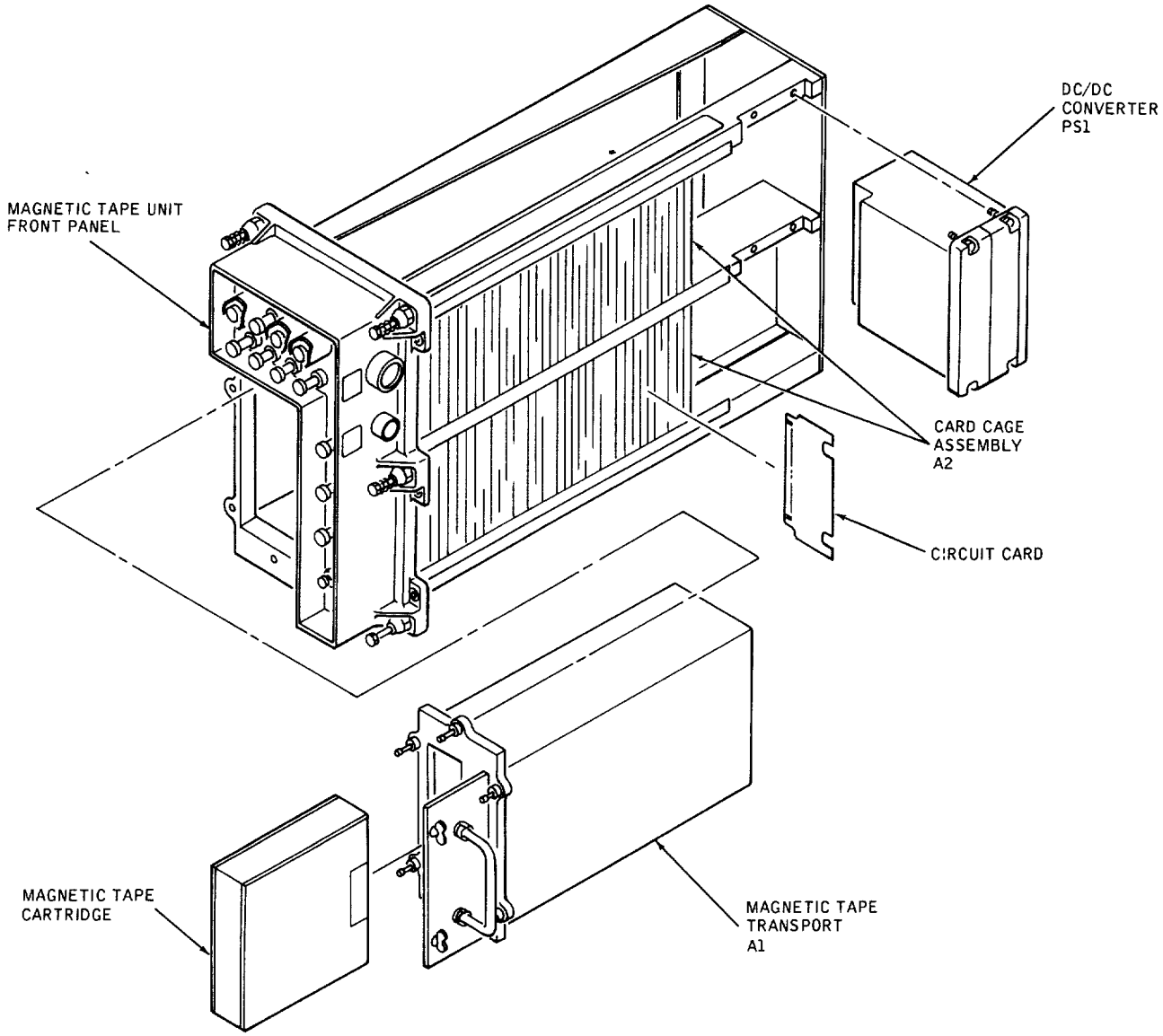
↔ Indicates bidirectional signal flow.

c. Equipment Interface. The troubleshooting diagrams may reference inputs and outputs interfacing between other pieces of equipment. When a notation shows that external equipment is involved, it is assumed that the user will refer to the applicable troubleshooting information provided for that equipment.

d. Logic Symbols. Logic symbols depend on card types. For discrete circuit cards containing conventional integrated circuits, conventional logic symbols are used. These symbols are used independently, with card locations and card pin numbers notated with the symbol. For analog circuits, circuit card details are provided only to functional level.

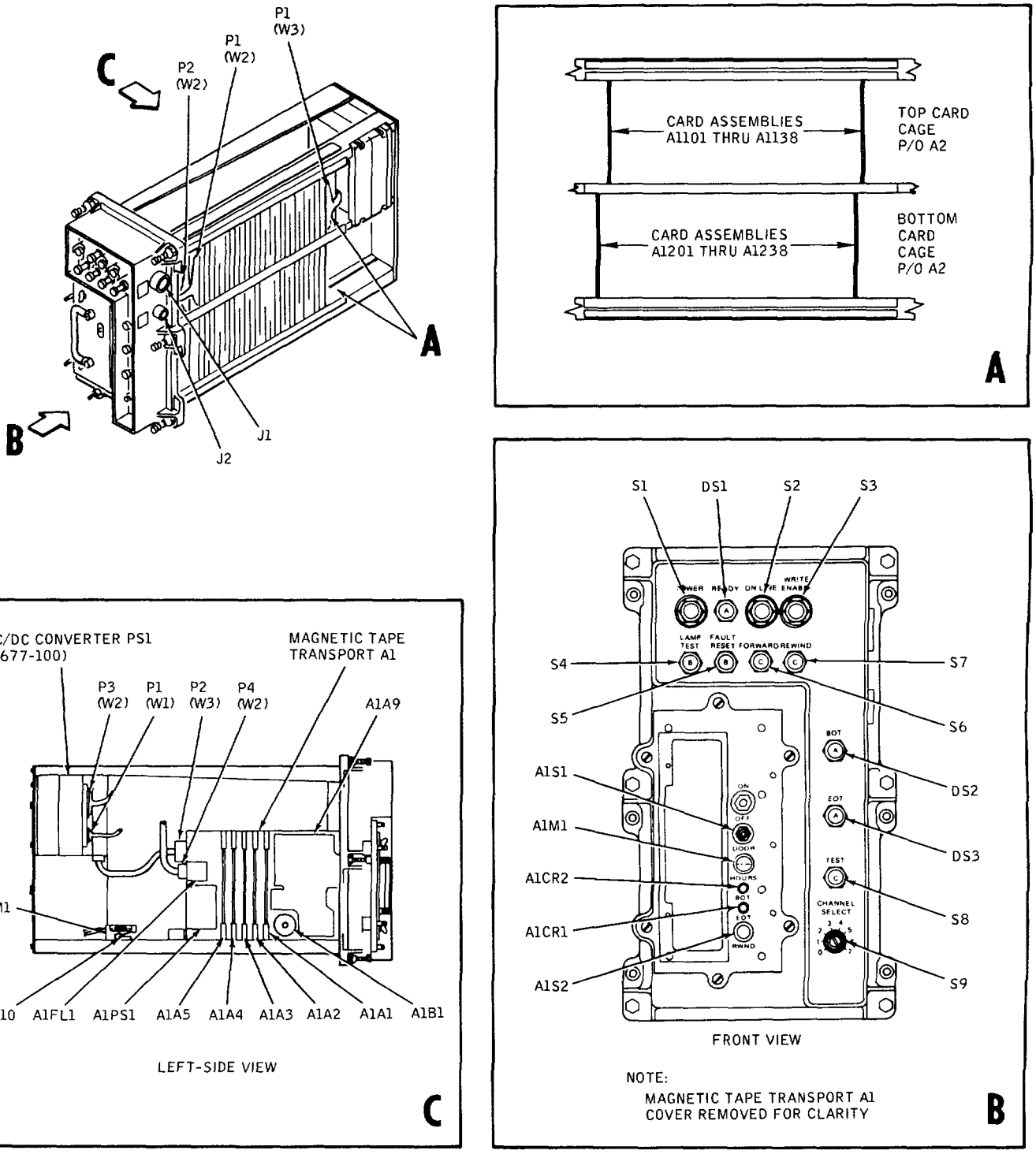
5-4. Physical Description (fig. 5-1). The MTU includes magnetic tape transport Al and an associated tape cartridge, card cage assembly A2, dc/dc converter PS 1, and a front-panel assembly containing switches, indicators, and external interface connectors. Locations and reference designations of major components of the MTU are shown in figure 5-2. The MTU major subassemblies are described in the following subparagraphs.

a. Front Panel Assembly (fig. 5-2). The front panel assembly contains all controls and indicators required for operation of the MTU. The controls and indicators permit the operator to place the MTU under automatic data processor (ADP) control, enable the write logic, advance or rewind the tape, enable the fault-detect logic, and perform self-test operations. External interface to the MTU is provided through device exchange channel (DEC) connector J 1 and POWER connector J2 mounted on the right side of the front-panel assembly. Connector J1 provides signal connections between the MTU and ADP and also provides an interlock that makes sure that the interconnecting cable is terminated. Connector J2 provides dc power connections between the MTU and the power cabinet through the maintenance bench power duct and an external power cable.



MS 197058

Figure 5-1. MTU Major Subassemblies.



MS 197066

Figure 5-2. MTU Component Location.

b. Magnetic Tape Transport Al and Cartridge (fig. 5-1). The magnetic tape transport (MTT) is a self-contained tape transport unit consisting basically of the tape-movement mechanism, read/ write/erase tape heads, motor control circuit card, read/write circuit card, and control logic circuit cards. The MTT is installed in the MTU through the front-panel assembly and is secured to the front panel by six captive screws. Connectors Jl and J2 are provided at the rear of the MTT for power and signal interface with MTU connectors W2P4 and W3P2, respectively (fig. 5-2). These connectors are accessible from the left side of the MTU when the slide-mounted frame is extended from the maintenance bench. The magnetic tape cartridge is installed and removed from the MTT through the spring-loaded access door on the front panel. Front panel controls and indicators are also accessible when the access door is in the open position. The tape cartridge consists of a tape supply and take-up reel, magnetic tape, and a tapetension mechanism. A write/protect cam is located on the front of the cartridge to prevent inadvertent destruction of recorded data.

c. Card Cage Assembly A2 (fig. 5-1). Included in card cage assembly A2 are two card shelves on a common wirewrap plane, with each shelf containing 32 digital circuit cards. The card cage and other MTU subassemblies are interconnected through ribbon-type cables W2 and W3 (fig. 5-2), the connectors of which connect to assigned card slots. Card cage assembly A2 is accessible from the right side of the MTU when the slide-mounted frame is extended from the maintenance bench.

d. DC/DC Converter PS1 (fig. 5-1). Dc/dc converter PS1 is installed in the upper-rear corner of the frame assembly and is secured with four mounting screws that are accessible from the right side of the MTU. Connectors J 1 and J2 are provided at the rear of the dc/dc converter for interface with MTU connectors W2P3 and WIPI, respectively (fig. 5-2). These connectors are accessible from the left side of the MTU when the slide-mounted frame is extended from the maintenance bench.

e. MTU Cabling. Figure 5-3 provides an overall cabling diagram for the MTU and illustrates the internal interconnection of wiring harnesses and cable assemblies contained in the MTU.

f: Circuit Card Location. Positions for circuit card assemblies within card cage assembly A2 are shown in figure 5-2. The MTU circuit card complement and locations are specified in TM 9-1430-65520-5.

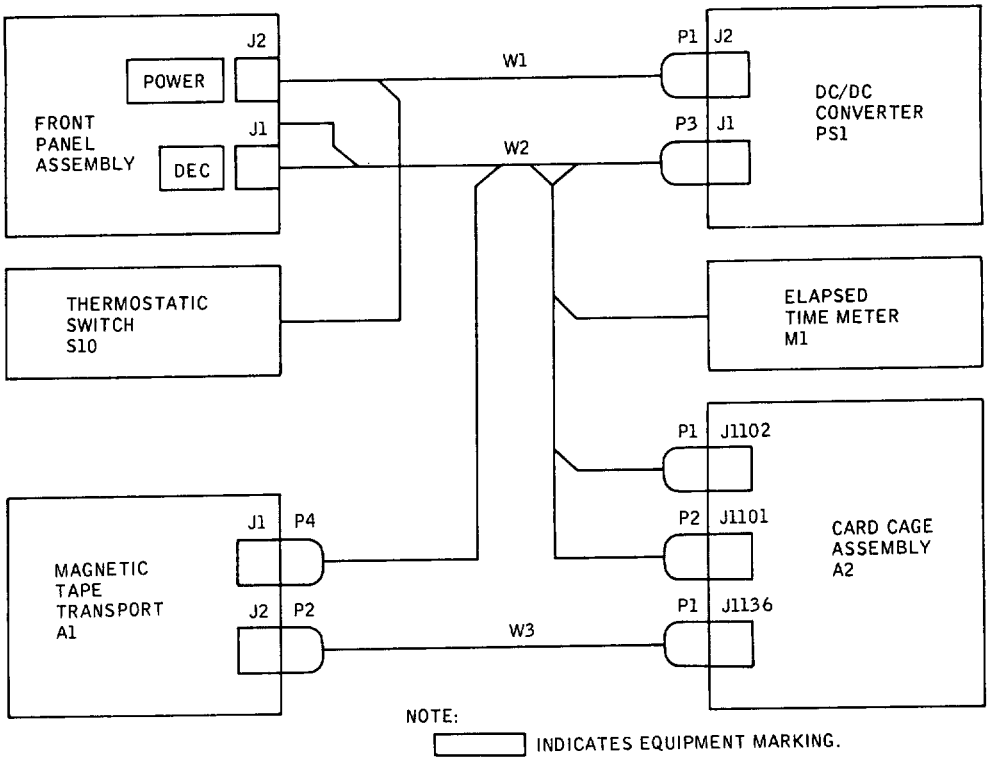
5-5. Circuit Card Location Index Tables and Key Signal Lookup Tables. Circuit card location index tables and key signal lookup tables provide figure references to functional logic diagrams. They permit rapid location of circuit areas corresponding to circuit card locations or signal mnemonics.

a. Card Location in Index. Table 5-1 shows the circuit card slots for the subassemblies of the MTU. This table provides figure and sheet references to the logic diagrams for specific circuit cards. Since often a card is used for various functional applications, certain cards have several figure references. The card location in logic diagrams index also indicates if a card can be tested by the MTS.

b. Key Signal Lookup. Table 5-2 lists the key signal lookup for the subassemblies of the MTU. Key signals are interconnecting signals going between physical assemblies or functional circuit areas as defined by the logic diagrams. Key signals are listed in alphanumerically order. The columns under the distribution heading list the foldout numbers and sheet number of each occurrence of the signal and the associated connector and pin number at which the signal is located on the foldout. They appear as follows:

1100 121O41

The first number is the foldout number (foldouts are located in volume 3). The first two digits are the foldout number and the last two digits are the sheet number. On a foldout with only one sheet, the last two digits are zeros. The second number is the connector and pin. Without a letter prefix, this is a card connector. An A prefix indicates an assembly connector, an X prefix indicates a socket, and a W prefix indicates a cable connector. An asterisk (*) before the connector indicates the source of the signal.



MS 197095

Figure 5-3. MTU Cabling Diagram.

Table 5-1. Card Location in Logic Diagrams Index

Card Slot	FO Sheet		
1101	0301	0302	0800
	1201	1802	2000
	2501	2502	
1102	0301	0302	1002
	1202	1802	1900
	2000	2501	2502
	2700		
1104	0100	0302	1202
	2102	2502	2700
1105	0301	0302	0800
	1002	1202	1802
	1900	2000	2501
1106	0301	2700	
1107	0301		
1108	0302		
1109	0302		
1110	0302		
1111	0302		
1112	0301	2700	
1113	0301	0302	0500
	1002	1202	1802
	1900	2000	
1114	0301	0302	1002
	1202	1802	1900
	2000		

Table 5-1. Card Location in Logic Diagrams Index - Continued

Card Slot	FO Sheet		
1115	0100	0301	0800
	0901	1202	1700
	1802	2000	2700
1116	0301	0302	0500
	0600	0800	0901
	0902	1700	
1117	0600	0700	0901
	0902	1700	2000
1118	0600	0700	0901
	1700	2000	
1119	0600	0700	0901
	0902	1700	2000
1120	0100		
1121	0302	0500	0600
1122	0301	0302	0600
1123	0500		
1124	1201	1202	1400
	1600	1700	1801
	1802		
1125	0400	1001	1201
	1802		
1126	1201	1400	1500
	1600	1801	1802
1127	0400	1201	1202
	1300	1500	1600

Table 5-1. Card Location in Logic Diagrams Index - Continued

Card Slot	FO Sheet		
	1801	1802	
1128	0400	0600	0800
	1500		
1129	0400	0800	1500
1130	0400	1001	1201
	1202	1400	1500
	1600	1801	
1131	1400	1500	1801
1132	1300	1400	1500
1133	0400	1001	1002
	1100	1201	1202
	1300	1400	1500
	1801	1900	2101
	2700		
1134	1201	1202	1400
	1500	1600	1801
	2102		
1135	0100	1001	1201
	1300	1802	1900
	2000	2101	2102
	2700		
1136	1001	1002	1201
	1202	1300	1400
	1900	2101	2102
	2700		
1202	0200	0600	1100

Table 5-1. Card Location in Logic Diagrams Index - Continued

Card Slot	FO Sheet		
	1201	1400	
1203	0200	0600	1100
	1201	1400	
1204	0200	0600	1100
	1201	1400	
1205	0200	0600	1100
	1201	1400	
1206	0100	0200	0600
	1100	1201	1400
1207	0100	0500	0600
	1802		
1208	0100	0200	0500
	0600	0800	0901
	1001	1700	1802
	2000		
1209	0100	0200	0500
	0600	0800	0901
	1700	1802	2000
1210	0200	0700	1100
1211	0200	0301	0500
	1100		
1212	0200	0302	0800
	1100		
1213	0301	0600	0800
	0901	1001	1100
	1700	1802	2000

Table 5-1. Card Location in Logic Diagrams Index - Continued

Card Slot	FO Sheet		
1214	0301	0600	0700
	0800	0901	1001
	1002	1201	1802
	2000		
1215	0800	6901	0902
	1001	1700	
1216	0800	0901	0902
	1 802		
1217	0600	0700	0901
	1001	1002	1600
	1802		
1218	0600	0800	0901
	0902	1001	
1220	1001	1002	
1221	0901	1001	1002
	1201	1802	2000
1222	0302	1001	1002
	1201	1400	1900
	2000		
1223	0500	1001	1002
	1201	1700	1900
	2000		
1224	0500	0700	1001
	1002	1202	1802
	2000		
1225	0500	1001	1002

Table 5-1. Card Location in Logic Diagrams Index - Continued

Card Slot	FO Sheet		
	1202	1600	
	1802	2000	
1226	1001	1201	1202
	1600	1801	
1227	1001	1002	1202
	1600	1900	2000
1228	0302	1001	1002
	1201	1202	1400
	1600	1900	
1229	0901	1001	1201
	1202	1400	1600
	1900	2000	
1230	1001	1201	1400
	1600	1801	
1231	1201	1202	1400
	1500	1900	
1232	1201	1400	
1233	1500	1801	
	1812	0600	

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
DEVIN1	0302	1102-13	0302	1104-13	2502	1102-13
	2502	*PS1J1-14	2502	W2PI-13	2502	W2P3-14
	2700	1102-13	2700	1104-13		
DEVINH	0302	*1104-14	0302	1121-05	0302	1121-10
	0302	1121-13	0302	1121-18	0302	1121-25
	0302	1121-26	0302	1121-34	0302	1121-42
	0302	1121-56	0600	1121-37	0600	1213-49
	0700	1224-10	2700	1104-14		
LOGOR1	2502	1102-39	2502	1104-40	2502	*PS1J1-16
	2502	W2P1-39	2502	W2P3-16	2700	1102-39
	2700	1104-40				
MTSGR	2700	1104-01	2700	1104-02	2700	1104-03
	2700	*1104-04				
SENVL1	2700	1104-45	2700	*1106-28		
SENVL2	2700	1104-39	2700	1104-43	2700	1104-65
	2700	*1112-24				
T003MA	0200	*1208-38	0200	1210-15		
T003MO	0200	*1210-10	1600	1127-68		
T005MA	0200	*1208-30	0200	1210-21		
T005MO	0200	*1210-19	1001	1224-03		
TO1 2MA	0200	1210-27	0200	*1211-23		
T015MA	0200	1210-38	0200	*1211-33		
T01 8SA	0200	1210-47	0200	*1211-45		
T01 8S0	0200	*1210-49	1802	1225-72		
T020MA	0200	*1208-33	0200	1210-35		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
T020M0	0200	*1210-37	1600	1225-68		
T023MA	0200	1210-36	0200	*1211-21	1600	1126-77
T040M0	0200	*1210-34	1001	1217-19	1001	1220-49
	1001	1220-62				
T047UA	1100	1133-74	1100	*1211-57		
T047UO	1100	*1133-72	1201	1232-08	1202	1134-36
T048UA	1100	1210-50	1100	*1211-69		
T048UO	1100	*1210-48	1202	1229-35		
TO4MHJ	0100	*1120-33	0100	1206-60	0100	1207-60
T050MA	0200	*1208-52	0200	1210-29		
T050MO	0200	*1210-30	1002	1225-54		
T060MA	0200	*1208-46	0200	1210-33		
T075MO	0200	*1210-40	1201	1226-19		
T075UA	0200	1210-09	0200	*1211-35		
T075UO	0200	*1210-07	1600	1226-73		
T080MO	0200	*1210-31	0901	1221-25	1001	1221-19
	1201	1127-11				
T150MA	0200	1210-39	0200	*1211-47		
T1 50MO	0200	*1210-42	1001	1221-73	1802	1225-79
T16MHA	0100	1120-47	0100	*1120-48	0100	1120-60
T16MHO	0100	*1120-51	0600	1117-70	0600	1118-70
	0600	1119-70	0700	1118-72	0700	1118-79
	0700	1119-72	0700	1119-79		
T16MIO	0100	*1120-54	0600	1202-10	0600	1203-10
	0600	1204-10	0600	1205-10	0600	1206-10
	2000	1227-05				

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
T390UA	1100	1210-41	1100	*1211-76		
T390U0	1100	*1210-46	1201	1225-47		
T4549A	1100	1133-69	1100	*1211-59		
T45490	1100	*1133-70	1202	1134-03	1202	1134-04
	1202	1134-08	1202	1134-11	1202	1134-17
	1202	1134-18	1202	1134-23	1202	1134-24
	1202	1134-40				
T900MA	0200	*1208-45	0200	1210-52		
TADS1AR	2102	*1136-43	2102	A1OA1-J1	2102	A1J2-71
	2102	W3P1-43	2102	W3P2-71	2102	XA4-21
	2700	W3P1-43	2700	W3P1-44	2700	W3P2-71
	2700	W3P2-72				
TBKK1A	1700	1208-23	1700	*1213-50		
TBOTOA	1900	*1222-39	1900	1228-74		
TBOTOR	1001	1221-72	1400	1230-19	1900	*1227-69
	1900	1227-69	1900	1228-65		
TBOTOS	0500	1123-35	0500	1123-53	1001	1222-41
	1001	1223-13	1900	1113-68	1900	1227-65
	1900	1227-78	1900	*1228-69	1900	1228-69
	1900	1229-62	1900	1229-75		
TBOT1 A	1900	1227-74	1900	*1231-76		
TBOT1R	1900	1228-59	1900	*1229-55	1900	1231-78
TBOT1S	1001	1213-65	1900	1227-29	1900	*1228-63
	1900	1228-63	1900	1229-53		
TBOT2A	1900	1228-61	1900	*1229-73		
TBOT2R	1900	*1227-80	1900	1228-76	1900	1229-77

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TBOT2S	1900	1223-59	1900	1227-76	1900	*1228-80
TBOT3A	1900	*1222-63	1900	1229-60		
TBOT4A	1900	*1227-33	1900	1228-78		
TBOTCO	1002	1222-49	1900	*1133-63	1900	1133-63
	1900	1222-35				
TBOTIB	1900	1102-75	1900	1105-65	1900	*1113-66
	1900	*1114-66	1900	W2DS2-02	1900	W2P1-75
	2501	1102-75	2501	W2DS-02	2501	W2P1-75
TBOTIBR	0301	1102-76	0301	1106-32	2501	1102-76
	2501	W2P1-76	2501	*W2S6-06		
TBOTID	1900	1105-65	1900	*1113-66		
TBOTJD	1900	1105-65	1900	*1114-66		
TBSYOA	1001	*1220-23	1001	1222-07	1001	1228-13
TBSY1A	1001	1220-20	1001	*1223-09		
TBSY2A	1001	1220-22	1001	*1223-15		
TBUSYR	0901	1215-26	0901	1218-10	1001	1213-59
	1001	*1221-11	1001	1222-03	1001	1230-73
TBUSYS	1001	1221-06	1001	1221-49	1001	1221-77
	1001	*1222-09	1001	1224-70	1002	1220-31
	1002	1224-56				
TCOOBP	0200	*1202-21	0200	1211-40		
TCOOBQ	0200	*1202-19	0200	1203-18	0200	1212-43
TC01BQ	0200	*1203-19	0200	1204-18		
TC02BQ	0200	*1204-19	0200	1205-18		
TC03BQ	0200	*1205-19	0200	1206-18		
TC04BP	0200	1202-18	0200	*1206-21	0200	1210-65

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
	0200	1211-42				
TC04BQ	0200	*1206-19	0200	1212-46		
TC10BQ	0200	*1202-37	0200	1203-40	0200	1212-48
TC11BQ	0200	*1203-37	0200	1204-40	0200	1211-37
TC12BP	0200	*1204-35	0200	1211-38		
TC12BQ	0200	*1204-37	0200	1205-40		
TC13BQ	0200	*1205-37	0200	1206-40		
TC14BP	0200	1202-40	0200	*1206-35	0200	1210-79
TC14BQ	0200	*1206-37	0200	1212-49		
TC20BQ	0200	*1202-31	0200	1203-34	0200	1212-50
TC21BQ	0200	*1203-31	0200	1204-34		
TC22BQ	0200	*1204-31	0200	1205-34		
TC23BQ	0200	*1205-31	0200	1206-34		
TC24BP	0200	1202-34	0200	*1206-33	0200	1210-73
TC24BQ	0200	*1206-31	0200	1212-52		
TC30BP	0200	*1202-47	0200	1208-34	0200	1211-34
TC30BQ	0200	*1202-49	0200	1203-54	0200	1211-19
	0200	1212-55				
TC31BP	0200	*1203-47	0200	1211-25		
TC31BQ	0200	*1203-49	0200	1204-54		
TC32BP	0200	*1204-47	0200	1208-40		
TC32BQ	0200	*1204-49	0200	1205-54	0200	1211-26
TC33BQ	0200	*1205-49	0200	1206-54	0200	1208-42
TC34BP	0200	1202-54	0200	*1206-47	0200	1208-36
	0200	1210-69	0200	1211-36		
TC34BQ	0200	*1206-49	0200	1211-20	0200	1212-60

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TC40BP	0200	*1202-45	0200	1208-54	0200	1211-22
	0200	1211-54				
TC40BQ	0200	*1202-43	0200	1203-48	0200	1211-30
	0200	1212-61				
TC41 BP	0200	*1203-45	0200	1208-29	0200	1211-31
TC41 BQ	0200	*1203-43	0200	1204-48	0200	1211-24
TC42BQ	0200	*1204-43	0200	1205-48	0200	1208-31
	0200	1208-48				
TC43BP	0200	*1205-45	0200	1208-50	0200	1211-14
TC43BQ	0200	*1205-43	0200	1206-48		
TC44BP	0200	1202-48	0200	*1206-45	0200	1208-56
	0200	1210-74	0200	1211-56		
TC44BQ	0200	*1206-43	0200	1211-18	0200	1212-62
TC5OBP	0200	*1202-59	0200	1211-49		
TC50BQ	0200	*1202-61	0200	1203-68	0200	1212-64
TC51BQ	0200	*1203-61	0200	1204-68	0200	1211-52
TC52BQ	0200	*1204-61	0200	1205-68	0200	1211-48
TC53BP	0200	*1205-59	0200	1211-50		
TC53BQ	0200	*1205-61	0200	1206-68	0200	1208-41
TC54BP	0200	1202-68	0200	*1206-59	0200	1208-43
TC54BQ	0200	1202-60	0200	1203-60	0200	*1206-61
	0200	1212-66				
TC60BP	0200	*1202-57	0200	1211-43	1802	1221-64
TC60BQ	0200	*1202-55	0200	1203-62	0200	1212-68
TC61 BP	0200	1202-62	0200	*1203-57		
TC61BQ	0200	*1203-55	0200	1209-19	0200	1211-46

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TC70BQ	1100	*1202-78	1100	1203-77	1100	1212-71
TC71BQ	1100	*1203-78	1100	1204-77	1100	1211-62
TC72BP	1100	*1204-76	1100	1211-64		
TC72BQ	1100	*1204-78	1100	1205-77	1100	1211-73
TC73BP	1100	*1205-76	1100	1211-74		
TC73BQ	1100	*1205-78	1100	1206-77		
TC74BP	1100	1202-77	1100	*1206-76	1100	1210-75
	1100	1211-70				
TC74BQ	1100	*1206-78	1100	1212-72		
TC80BQ	1100	*1202-74	1100	1203-71	1100	1212-73
TC81BQ	1100	*1203-74	1100	1204-71		
TC82BQ	1100	*1204-74	1100	1205-71		
TC83BP	1100	*1205-69	1100	1211-55	1100	1211-66
	1100	1211-71				
TC83BQ	1100	*1205-74	1100	1206-71	1100	1211-78
TC84BP	1100	1202-71	1100	*1206-69	1100	1211-79
TC84BQ	1100	1204-60	1100	12r--60	1100	*1206-74
	1100	1211-60	1100	1211-68	1100	1211-72
	1100	1212-74				
TC90BQ	1100	*1204-55	1100	1205-62	1100	1211-75
	1100	1212-75				
TC91BP	1100	1204-62	1100	*1205-57	1100	1211-77
TC91BQ	1100	*1205-55	1100	1212-77		
TCCPOO	0200	1202-14	0200	1203-14	0200	1204-14
	0200	1205-14	0200	1206-14	0200	*1209-21

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TCCP10	0200	1202-42	0200	1203-42	0200	1204-42
	0200	1205-42	0200	1206-42	0200	*1210-68
TCCP20	0200	1202-30	0200	1203-30	0200	1204-30
	0200	1205-30	0200	1206-30	0200	*1210-80
TCCP30	0200	1202-56	0200	1203-56	0200	1204-56
	0200	1205-56	0200	1206-56	0200	*1210-71
TCCP40	0200	1202-46	0200	1203-46	0200	1204-46
	0200	1205-46	0200	1206-46	0200	*1210-70
TCCP50	0200	1202-70	0200	1203-70	0200	1204-70
	0200	1205-70	0200	1206-70	0200	*1210-72
TCCP70	1100	1202-79	1100	1203-79	1100	1204-79
	1100	1205-79	1100	1206-79	1100	*1210-78
TCCP80	1100	1202-72	1100	1203-72	1100	1204-72
	1100	1205-72	1100	1206-72	1100	*1210-77
TCDERD1	1802	*1114-33	1802	1135-42		
TCDERO	1802	1207-34	1802	*1213-80		
TCDERP	1802	*1207-33	1802	1213-78	1802	1217-75
TCDERQ	0500	1123-77	1802	1114-29	1802	*1207-31
TCRSOA	0200	*1210-66				
TCRSOB	0200	1202-17	0200	1202-29	0200	1202-39
	0200	1202-41	0200	1202-51	0200	1202-53
	0200	1202-63	0200	1203-17	0200	1203-29
	0200	1203-39	0200	1203-41	0200	1203-51
	0200	1203-53	0200	1203-63	0200	1204-17
	0200	1204-29	0200	1204-39	0200	1204-41
	0200	1204-51	0200	1204-63	0200	1205-17

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
	0200	1205-29	0200	1205-39	0200	1205-41
	0200	1205-51	0200	1205-63	0200	1206-17
	0200	1206-29	0200	1206-39	0200	1206-41
	0200	1206-51	0200	1206-63	0200	*1210-56
	0200	*1210-63	0200	*1210-66		
TCRSOO	0200	1210-55	0200	1210-61	0200	1210-64
	0200	*1212-35				
TCRS1A	0200	*1210-63				
TCRS2A	0200	*1210-56				
TCRS7A	1100	1202-65	1100	1202-80	1100	1203-65
	1100	1203-80	1100	1204-53	1100	1204-65
	1100	1204-80	1100	1205-53	1100	1205-65
	1100	1205-80	1100	1206-65	1100	1206-80
	1100	*1210-60				
TCRS70	1100	1210-62	1100	*1213-64		
TCRSCA	0200	1212-37	1500	*1127-80		
TCZROA	0200	1210-51	0200	*1212-47		
TCZROO	0200	*1210-53	1001	1221-48	1001	1224-59
	1001	1225-11	1002	1225-59	1201	1127-35
TCZR1A	0200	1210-45	0200	*1212-59		
TCZR10	0200	*1210-43	0200	1212-54		
TCZR7A	1100	1210-59	1100	*1212-76		
TCZR70	1100	*1210-57	1201	1229-47	1202	1229-30
TDBFBP	1201	1232-46	1201	1232-61	1400	1130-77
	1400	*1131-57				
TDBFRA	1400	*1130-57	1400	1131-64		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TDBFRO	1400	1130-53	1400	*1231-47		
TDCPOO	0400	1128-01	0400	1128-10	0400	1128-14
	0400	1128-26	0400	1128-70	0400	*1130-'38
TDCP10	0400	1128-30	0400	1128-42	0400	1128-46
	0400	1128-56	0400	*1130-30	1400	1131-60
	1802	1207-30				
TDIR10	0901	*1115-24	0901	1118-24		
TDIRCA	1002	*1133-53	1002	1136-47	2101	A10A1-F1
	2101	A1J2-53	2101	W3P2-53	2101	XA4-31
	2700	W3P1-47	2700	W3P2-53		
TDIRCAR	2101	*1133-44	2101	1136-48	2101	A1OA1-E1
	2101	A1J2-54	2101	W3P2-54	2700	W3PI-48
	2700	W3P2-54				
TDIRIR	1001	1213-71	1002	1113-78	1002	1217-60
	1002	1217-66	1002	1222-47	1002	1222-68
	1002	*1223-66				
TDIRIS	1001	1213-77	1002	1113-74	1002	1133-51
	1002	1217-46	1002	1217-52	1002	*1222-66
	1002	1223-18	1002	1223-68		
TDIRSP	0901	*1118-23	1001	1223-11	1002	1217-55
	1002	1217-61	1002	1227-62		
TDIRSQ	0901	*1118-25	1001	1223-03	1002	1217-43
	1002	1217-49	1002	1227-68		
TDOOBQ	0400	*1128-13	0400	1129-08		
TDO1BQ	0400	*1128-07	0400	1129-05		
TDO2BQ	0400	*1128-25	0400	1129-24		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TD03BQ	0400	*1128-19	0400	1129-18		
TDOLBQ	0400	*1128-37	0400	1129-40		
TDO5BQ	0400	*1128-31	0400	1129-34		
TD06BQ	0400	*1128-49	0400	1129-54		
TD07BQ	0400	*1128-43	0400	1129-48		
TDOPBO	0400	*1128-61				
TDOPBQ	0400	1129-68				
TDRIOA	1002	1222-70	1002	*1227-66		
TDRI1A	1002	1223-70	1002	*1227-60		
TDRSOA	0400	1128-04	0400	1128-06	0400	1128-20
	0400	1128-22	0400	1128-66	0400	*1133-80
TDRSOO	0400	*1127-27	0400	1133-73	0400	1133-79
	1400	1232-20				
TDRS1A	0400	1128-36	0400	1128-38	0400	1128-50
	0400	1128-52	0400	*1133-71		
TDRSCA	0400	1127-21	1500	*1231-09		
TDSCOA	1001	1221-78	1002	*1214-39		
TDSCOO	1002	1214-35	1002	1220-36	1002	*1221-59
TDSC1A	1002	*1217-47	1002	1221-61		
TDSC2A	1002	*1217-45	1002	1221-66		
TDSC3A	1002	*1217-59	1002	1221-68		
TDSC4A	1002	*1217-57	1002	1221-70		
TEB09A	1700	1115-20	1700	*1116-01		
TEB090	1700	*1115-18	1700	1117-18		
TEBOBP	1700	1116-04	1700	*1117-21	1700	1215-14
TEBOSA	1700	*1116-22	1700	1117-17		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TEB19A	1700	1115-17	1700	*1116-06		
TEB190	1700	*1115-14	1700	1118-18		
TEBLBP	1700	1116-08	1700	*1118-21	1700	1215-18
TEB1BQ	1700	1117-14	1700	*1118-19		
TEBISA	1700	*1116-14	1700	1118-17		
TEB29A	1700	1115-21	1700	*1124-69		
TEB290	1700	*1115-19	1700	1119-18		
TEB2BP	1700	*1119-21	1700	1124-65	1700	1215-19
TEB2BQ	1700	1118-14	1700	*1119-19		
TEB2SA	1700	*1116-21	1700	1119-17		
TEB390	1700	*1115-26	1700	1118-40		
TEB3BP	1700	*1118-35	1700	1215-20		
TEB3BQ	1700	1115-27	1700	*1118-37	1700	1119-14
TEB3SA	1700	*1116-27	1700	1118-39		
TEBCPA	1700	1118-42	1700	*1209-27		
TEBCPO	1700	*1208-27	1700	1209-23		
TEBRSA	0901	*1214-66	1700	1117-20	1700	1118-20
	1700	1118-38	1700	1119-20		
TEBZRA	1700	111'5-59	1700	1209-25	1700	*1215-21
TEBZRO	1201	1231-35	1400	1231-40	1600	1217-38
	1700	*1115-57				
TEOTOA	1900	*1222-52	1900	1228-79		
TEOTOR	1400	1230-20	1900	*1227-75	1900	1227-75
	1900	1228-77				
TEOTOS	0500	1123-41	0500	1123-59	1001	1223-07
	1900	1113-62	1900	1227-73	1900	1227-77

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
	1900	*1228-75	1900	1228-75	1900	1229-65
	1900	1229-70				
TEOT1A	1900	1227-79	1900	*1231-69		
TEOT1 R	1900	1228-53	1900	*1229-64	1900	1231-73
TEOT1S	1001	1213-75	1900	1227-35	1900	*1228-57
	1900	1228-57	1900	1229-66		
TEOT2A	1900	1228-55	1900	*1229-74		
TEOT2R	1900	*1227-72	1900	1228-71	1900	1229-71
TEOT2S	1900	1227-40	1900	1227-71	1900	*1228-72
TEOT3A	1900	*1227-38	1900	1229-68		
TEOT4A	1900	*1227-39	1900	1228-73		
TEOTCO	1002	1223-20	1900	*1133-60	1900	1133-60
	1900	1222-54				
TEOTIB	1900	1102-77	1900	1105-63	1900	*1113-60
	1900	*1114-60	1900	W2DS3-02	1900	W2P1-77
	2501	1102-77	2501	W2DS3-02	2501	W2P1-77
TEOTIBR	0301	1102-78	0301	1106-32	2501	1102-78
	2501	W2P1-78	2501	*W2S8-06		
TEOTID	1900	1105-63	1900	*1113-60		
TEOTJD	1900	1105-63	1900	*1114-60		
TERCIA	0901	*1221-23	1001	1220-04		
TERROA	1802	*1115-42	1802	1207-36	1802	1207-38
	1802	1207-50	1802	1207-52	1802	1207-66
	1802	1207-75				
TERROO	1802	1115-39	1802	*1217-33		
TERRIB	1802	1102-29	1802	1102-69	1802	1105-78

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
	1802	*1113-63	1802	*1114-63	1802	W2P1-29
	1802	W2P3-32	1802	W2S5-08	2501	1102-29
	2501	1102-69	2501	W2P1-29	2501	W2P1-69
	2501	W2P3-32	2501	W2S5-08		
TERRIBR	0301	1102-70	0301	1106-16	2501	1102-70
	2501	W2P1-70	2501	*W2S4-05		
TERRID	1802	1105-78	1802	*1113-63		
TERRJD	1802	1105-78	1802	*1114-63		
TERSFP	0901	*111 8-11	1201	1130-70	1202	1127-60
	1802	1221-31				
TERSFQ	0901	*1118-13	0901	1221-22		
TERSRP	0901	*1118-09	0901	1229-61	1202	1127-62
TERST04	1802	1101-70	1802	1105-25	1802	1208-05
	1802	W2P2-70	1802	*W2S5-01	2501	1101-70
	2501	W2P2-70	2501	*W2S5-01		
TERSTA4	1802	1101-69	1802	1105-23	1802	1209-05
	1802	W2P2-69	1802	*W2S5-03	2501	1101-69
	2501	W2P2-69	2501	W2S5-03		
TERSTR	1802	*1208-01	1802	1209-04	1802	1217-30
TERSTS	1802	1208-04	1802	*1209-01		
TESF1A	0901	1115-06	0901	*1215-59	0901	1216-48
TESF10	0901	*1115-08	0901	1118-08		
TESR1A	0901	1115-05	0901	*1215-57	0901	1216-49
TESR10	0901	*1115-01	0901	1118-05		
TESTOQ	2000	1117-34	2000	*1119-37		
TEST1P	2000	*1117-33	2000	1225-29		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TEST1Q	2000	*1117-31	2000	1118-34		
TEST2Q	2000	*1118-31	2000	1119-34		
TEST30	2000	1114-11	2000	*1115-49		
TEST3Q	2000	1117-40	2000	*1119-31		
TEST40	2000	1114-18	2000	1114-24	2000	*1223-39
TEST4P	2000	*1117-35	2000	1118-56	2000	1119-40
	2000	1119-56				
TEST4Q	2000	*1117-37	2000	1225-30		
TEST5P	2000	*1118-47	2000	1223-29	2000	1223-54
TEST5Q	2000	*1118-49	2000	1119-54	2000	1223-48
	2000	1224-30	2000	1224-35	2000	1224-40
TEST6P	2000	1114-08	2000	1118-54	2000	*1119-47
	2000	1223-50	2000	1223-56		
TEST6Q	2000	*1119-49	2000	1223-31	2000	1224-34
	2000	1224-37	2000	1224-42		
TEST70	2000	1114-23	2000	*1115-48		
TESTDA	2000	1222-31	2000	1222-36	2000	*1223-33
	2000	1227-04				
TESTKA	2000	1117-30	2000	1117-42	2000	1118-30
	2000	1119-30	2000	1119-42	2000	*1227-01
TESTPO	2000	1114-40	2000	*1229-04		
TESTSA	2000	1115-41	2000	*1225-31		
TESTSO	2000	1114-10	2000	1114-13	2000	1114-20
	2000	1114-25	2000	1114-26	2000	1114-36
	2000	1114-42	2000	*1115-46		
TFLMPT1	2501	PS1J1-30	2501	W2P3-30	2501	W2S4-04

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
	2501	*W2S4-04				
TFLTOO	1802	1113-59	1802	*1217-76		
TFLT10	1802	1114-59	1802	*1217-69		
TFPE1A	1202	*1231-33	1802	1207-63		
TFPE2A	1001	1220-19	1202	*1130-72		
TFPERD1	1802	*1114-45	1802	1135-46		
TFPERP	1802	*1207-59	1802	1217-78		
TFPERQ	0500	1123-71	1802	1114-41	1802	*1207-61
TFPRSO	1201	*1133-57	1202	1226-42		
TFSTOA	1002	*1220-35	1002	1223-43		
TFSTOR	1002	1223-41	1002	*1224-50		
TFSTOS	1002	1222-55	1002	*1223-45	1002	1224-52
	1002	1225-57	1002	1228-04		
TFST1A	1002	1224-54	1002	*1228-66		
TFST1R	1002	*1222-57	1002	1223-53	1002	1228-05
	1002	1228-62				
TFST1S	1002	1222-53	1002	*1223-57	1002	1225-52
TFST2A	1002	1223-55	1002	*1225-63		
TFST2R	1002	1223-47	1002	*1224-43		
TFST2S	1002	*1223-51	1002	1224-41	1002	1228-68
TFST3A	1002	1224-46	1002	*1228-60		
TFST4A	1001	1226-50	1002	1223-49	1002	*1225-50
TFSTRA	0200	1212-34	1002	*1228-01		
TGAP10	1600	1225-06				
TGAP10	0901	*1229-63				
THISPP	0901	*1119-09	1001	1214-25	1001	1214-73

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
THISPQ	0901	*1119-07	0901	1213-53	1600	1230-43
THSCLA	0901	*1213-55	1001	1220-06		
THSGOA	0200	1212-40	1600	1125-73	1600 .	*1230-47
	1600	1230-47				
THSGOR	1600	1125-71	1600	*1126-74		
THSGOS	1600	*1125-72	1600	1126-65	1600	1127-66
THSG1A	1600	*1124-75	1600	1126-71		
THSG1R	1600	1125-77	1600	*1126-73	1600	1230-49
THSG1S	1600	1124-77	1600	*1125-75	1600	1126-75
THSG2A	0600	1812-62	1600	1125-79	1600	*1127-64
	1600	1127-64				
THSP1A	0901	1115-09	0901	1116-07	0901	*1213-43
	0901	121 6-50				
THSP10	0901	*1115-07	0901	1119-05		
TINT10	1001	1214-71	1001	1214-77	1001	*1220-11
TINT1A	1001	*1214-75	1001	1215-77	1001	1221-08
	1001	1224-11				
TINT2A	0500	1224-17	0600	1218-66	1001	*1214-72
	1001	1218-72				
TINT5A	1001	*1214-09	1001	1215-78	1001	1221-10
	1001	1224-13	1001	1226-26		
TINT50	1001	*1208-66	1001	1214-03	1001	1214-23
TINT6A	0500	1224-18	0600	1218-68	1001	*1214-27
	1001	1218-73				
TINT7A	1001	1208-68	1001	*1213-73	1201	1221-05
TINT9A	1001	1208-70	1001	*1213-74		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TKAOOP	1500	*1129-69	1500	1131-73	1500	1132-73
TKAO1P	1500	1126-57	1500	*1131-69	1500	1233-34
TKA01Q	1500	1127-69	1500	*1131-74	1500	1131-74
	1500	1132-71	1500	1231-04	1500	1231-08
	1500	1233-05	1801	1233-20		
TKA02P	1500	1127-76	1500	1128-72	1500	1129-72
	1500	1131-71	1500	*1132-69	1500	1231-05
	1500	1231-10				
TKA02Q	1500	1126-59	1500	*1132-74	1500	1132-74
	1500	1233-06	1500	1233-36	1801	1233-22
TKCOOP	1500	*1128-69	1500	1231-06		
TKCRSA	1500	1128-73	1500	*1133-68		
TKCRSO	1500	*1127-43	1500	1133-65		
TKRSOA	1500	1129-73	1500	*1130-69		
TKRSOO	1500	1130-65	1500	*1134-80		
TKRS10	1500	1130-76	1500	*1233-47		
TKRS1A	1500	*1130-80	1500	1134-78		
TLADOA	1001	1222-26	1001	*1225-15		
TLADOR	1001	1224-09	1001	*1225-07	1400	1126-76
TLADOS	1001	1223-17	1001	1223-26	1001	*1224-15
	1001	1225-01	1001	1225-09		
TLAD1A	1001	1225-03	1001	*1227-06		
TLAD1R	1001	1222-18	1001	1222-19	1001	1222-24
	1001	*1223-22				
TLAD1S	1001	*1222-22	1001	1223-24	1001	1224-01
TLAD2A	1001	1223-19	1001	*1224-07	1001	1229-11

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TLAD2R	1001	*1228-15	1001	1229-09		
TLAD2S	1001	1227-08	1001	1228-11	1001	*1229-15
	1001	1230-74				
TLAD3A	1001	*1222-14	1001	1224-23		
TLAD3R	1001	1223-17	1001	*1224-27		
TLAD3S	1001	*1223-21	1001	1224-21	1001	1224-53
TLADRA	0200	1212-36	1001	*1222-21		
TLATED1	1802	*1114-52	1802	1135-35		
TLATEP	1802	*1207-47	1802	1214-59	1802	1217-71
TLATEQ	0500	1123-54	1802	1114-54	1802	*1207-49
TLATSA	1201	1130-54	1801	*1233-23	1802	1207-51
TLCCOA	1201	1125-61	1201	*1231-23		
TLCCOR	1201	1125-59	1201	*1126-64	1201	1232-05
	1201	1232-31				
TLCCOS	1201	*1125-63	1201	1126-66	1201	1232-43
	1201	1232-55				
TLCC1A	1201	1126-68	1201	*1134-52	1201	1225-35
TLCC1R	1201	*1225-39	1201	1226-30		
TLCC1S	1201	1125-78	1201	1134-35	1201	1225-33
	1201	*1226-33	1201	1229-45		
TLCC2A	1201	1226-31	1201	*1232-47		
TLCC2R	1201	1124-76	1201	*1125-80	1201	1134-37
	1201	1134-48				
TLCC2S	1201	*1124-80	1201	1125-76	1201	1225-45
TLCC3A	1201	*1134-46	1201	1229-24		
TLCC3R	1201	1228-17	1201	*1229-20		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TLCC3S	1201	1134-54	1201	1214-55	1201	*1228-21
	1201	1229-22				
TLCC4A	1201	1124-78	1201	*1229-51		
TLCC6A	1201	*1225-51	1201	1228-19		
TLCC9A	1201	*1214-57	1201	1229-18		
TLMPTA1	1802	1217-74	2000	1102-79	2000	1115-55
	2000	1135-37	2000	W2P1-41	2000	W2P1-79
	2000	*W2S4-03	2501	1102-79	2501	W2P1-79
	2501	*W2S4-03				
TLMPTA1R	2501	1102-80	2501	W2P1-80	2501	*W2S4-06
TLMPTAR	0301	1102-80	0301	*1115-58		
TLMPTO	1002	1114-65	1002	1114-76	1202	1114-53
	1900	1114-62	1900	1114-68	2000	1113-49
	2000	1114-71	2000	1114-77	2000	*1115-56
TLNGED1	1802	*1114-46	1802	1135-39		
TLNGEP	1802	*1207-45	1802	1214-61	1802	1217-72
TLNGEQ	0500	1123-47	1802	1114-48	1802	*1207-43
TLNGSA	1201	1130-56	1801	*1226-76	1802	1207-41
TLPTOP	0901	*1117-47	1001	1218-75		
TLPTOQ	0901	*1117-49	0901	1118-48		
TLPT1A	0400	1127-18	0400	1127-26	0500	1224-26
	0600	1218-64	0901	*1116-33	0901	1117-56
TLPT1Q	0901	1116-29	0901	*1118-43		
TLRCOO	1801	1131-08	1801	*1133-14		
TLRCOQ	1801	*1131-13	1801	1133-17	1801	1230-55
TLRC10	1801	1131-05	1801	*1133-19		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TLRC1Q	1801	*1131-07	1801	1133-21	1801	1230-60
TLRC20	1801	1131-24	1801	*1133-26		
TLRC2Q	1801	*1131-25	1801	1133-27	1801	1230-61
TLRC30	1801	1131-18	1801	*1133-40		
TLRC3Q	1801	*1131-19	1801	1133-38	1801	1230-62
TLRC40	1801	1131-40	1801	*1133-37		
TLRC4Q	1801	*1131-37	1801	1133-35	1801	1230-64
TLRC50	1801	*1131-34	1801	1133-34		
TLRC5Q	1801	*1131-31	1801	1133-36	1801	1230-66
TLRC60	1801	1131-54	1801	*1133-30		
TLRC6Q	1801	*1131-49	1801	1133-29	1801	1230-68
TLRC70	1801	1131-48	1801	*1133-31		
TLRC7Q	1801	*1131-43	1801	1133-33	1801	1230-70
TLRCAA	1801	1130-48	1801	*1230-59		
TLRCAO	1801	*1130-46	1801	1134-43		
TLRCBA	1801	*1134-45	1801	1226-77		
TLRCPO	1801	1131-68	1801	*1133-42		
TLRCPQ	1801	*1131-61	1801	1133-39	1801	1134-41
TLRCRA	1100	1213-68	1201	*1134-39		
TLRCSA	1801	*1127-74	1801	1131-03	1801	1131-15
	1801	1131-17	1801	1131-27	1801	1131-29
	1801	1131-39	1801	1131-41	1801	1131-51
	1801	1131-63				
TMFWDA4	2000	1101-45	2000	1105-37	2000	1214-20
	2000	W2P2-45	2000	*W2S6-03	2501	1101-45
	2501	W2P2-45	2501	*W2S6-03		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TMFWD04	2000	1101-46	2000	1105-39	2000	1213-17
	2000	W2P2-46	2000	*W2S6-01	2501	1101-46
	2501	W2P2-46	2501	*W2S6-01		
TMFWDR	2000	*1213-19	2000	1214-18	2000	1223-36
	2000	1225-40				
TMFWDS	2000	1213-14	2000	*1214-14		
TMFWIB	1002	1102-63	1002	1105-73	1002	*1113-69
	1002	*1114-69	1002	W2S6-08	2501	1102-63
	2501	W2P1-63	2501	W2S6-08		
TMFWIBR	0301	1102-64	0301	1106-67	2501	1102-64
	2501	W2P1-64	2501	*W2S6-04		
TMFWID	1002	1105-73	1002	*1113-69		
TMFWJD	1002	1105-73	1002	*1114-69		
TMFWSR	2000	*1222-33	2000	1223-34		
TMFWSS	2000	1222-29	2000	*1223-30	2000	1224-29
TMRWIB	1002	1102-61	1002	1105-71	1002	*1113-80
	1002	*1114-80	1002	W2S7-08	2501	1102-61
	2501	W2P1-61	2501	W2S7-08		
TMRWIBR	0301	1102-62	0301	1106-67	2501	1102-62
	2501	W2P1-62	2501	*W2S7-04		
TMRWID	1002	1102-61	1002	1105-71	1002	*1113-80
TMRWJD	1002	1102-61	1002	1105-71	1002	*1114-80
TMRWNA4	2000	1101-41	2000	1105-46	2000	1214-26
	2000	W2P2-41	2000	*W2S7-03	2501	1101-41
	2501	W2P2-41	2501	*W2S7-03		
TMRWN04	2000	1101-42	2000	1105-35	2000	1213-24

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
	2000	W2P2-42	2000	*W2S7-01	2501	1101-42
	2501	W2P2-42	2501	*W2S7-01		
TMRWNR	2000	*1213-20	2000	1214-24	2000	1223-42
	2000	1225-38				
TMRWNS	2000	1213-22	2000	*1214-22		
TMRWSD	2000	1101-72	2000	*1113-52	2000	W2P2-72
	2000	W2S6-05	2000	W2S7-05	2501	1102-72
	2501	W2P2-72	2501	W2S6-05	2501	W2S7-05
TMRWSR	2000	*1222-30	2000	1223-40		
TMRWSS	2000	1222-34	2000	*1223-38	2000	1224-38
TMTESD	0800	W2S9A-C	2000	1101-73	2000	*1113-46
	2000	W2P2-73	2000	W2S8-05	2501	1101-73
	2501	W2P2-73	2501	W2S8-05		
TMTROA	2000	*1115-43	2000	1117-36	2000	1117-38
	2000	1118-36	2000	1118-52	2000	1119-36
	2000	1119-38				
TMTROO	2000	1115-45	2000	*1222-46		
TMTR1A	2000	*1115-53	2000	1119-52	2000	1222-50
TMTR10	2000	1115-51	2000	*1225-36		
TMTSIB	2000	1102-65	2000	1105-75	2000	*1113-72
	2000	*1114-72	2000	W2P1-65	2000	W2S8-08
	2501	1102-65	2501	W2P1-65	2501	W2S8-08
TMTSIBR	0301	1102-66	0301	1106-16	2501	1102-58
	2501	1102-66	2501	W2P1-58	2501	W2P1-66
	2501	*W2S8-02				
TMTSID	2000	1105-75	2000	*1113-72		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TMTSJD	2000	1105-75	2000	*1114-72		
TMTSSR	2000	*1221-35	2000	1222-40		
TMTSSS	2000	1113-71	2000	1221-37	2000	*1222-38
	2000	1224-33				
TMTSTA4	2000	1101-47	2000	1105-52	2000	1214-19
	2000	W2P2-47	2000	*W2S8-03	2501	1101-47
	2501	W2P2-47	2501	*W2S8-03		
TMTST04	2000	1101-48	2000	1105-48	2000	1213-23
	2000	W2P2-48	2000	*W2S8-01	2501	1101-48
	2501	W2P2-48	2501	*W2S8-01		
TMTSTR	2000	*1213-27	2000	1214-17	2000	1222-42
	2000	1225-42				
TMTSTS	2000	1213-21	2000	*1214-21		
TNDA1A	1802	1224-65	1802	*1225-73		
TNDA10	1802	1221-30	1802	*1224-74		
TNDA2A	1802	1224-71	1802	*1225-74		
TNDA3A	1802	*1221-57	1802	1224-72		
TNDATD1	1802	*1114-51	1802	1135-52		
TNDATP	1802	*1207-35	1802	1217-79		
TNDATQ	0500	1123-48	0500	1123-62	1802	1114-47
	1802	*1207-37				
TNDTSA	1001	1220-08	1802	1207-39	1802	*1221-33
TNSGOA	1500	*1231-11	1600	1227-55		
TNSGOR	1600	*1226-59	1600	1226-59	1600	1227-53
	1802	1225-77				
TNSGOS	1600	1226-61	1600	1226-71	1600	*1227-57

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TNSG1A	1600	1226-66	1600	*1228-09		
TNSG1R	1400	1230-24	1600	*1226-57	1600	1226-57
	1600	1227-59				
TNSG1S	1600	1225-66	1600	1226-55	1600	*1227-63
	1600	1228-03				
TNSG2A	1600	*1226-69	1600	1227-61		
TNSG2R	1600	1228-35	1600	1228-41	1600	*1229-50
TNSG2S	1600	1134-47	1600	1217-40	1600	1225-08
	1600	1225-60	1600	1227-23	1600	*1228-45
	1600	1228-45	1600	1229-52	1801	1226-78
TNSG3A	1600	1226-60	1600	*1227-27		
TNSG3R	1600	1228-47	1600	*1229-43		
TNSG3S	1600	1130-41	1600	*1228-51	1600	1229-41
TNSG4A	1600	*1225-64	1600	1228-43		
TNSG5A	1400	1230-34	1500	1127-46	1600	*1130-45
	1600	1130-45	1600	1229-54		
TNSG6A	1600	*1134-51	1600	1228-49		
TNSG7A	1600	*1228-39	1600	1229-46		
TNSGAA	1001	1220-01	1600	*1225-04		
TNSGCA	1600	*1225-55	1700	1208-25		
TONLIB	2000	1102-59	2000	1105-66	2000	*1113-51
	2000	W2P1-59	2000	W2S2-02	2501	1102-59
	2501	W2P1-59	2501	W2S2-02		
TONLIBR	0301	1102-60	0301	1106-32	2501	1102-60
	2501	W2P1-60	2501	*W2S2-04		
TONLNA4	2000	1101-37	2000	1105-29	2000	1208-10

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
	2000	W2P2-37	2000	*W2S2-03	2501	1101-37
	2501	W2P2-37	2501	*W2S2-03		
TONLN04	2000	1101-38	2000	1105-42	2000	1209-1
	2000	W2P2-38	2000	*W2S2-01	2501	1101-38
	2501	W2P2-38	2501	*W2S2-01		
TONLNR	2000	1208-08	2000	*1209-06	2000	1213-1 8
	2000	1213-25	2000	1213-26	2000	1225-34
TONLNS	0301	121 3-42	0500	121 1-01	0800	1213-13
	0800	1213-34	0800	1214-05	1201	1232-04
	1202	1226-37	1400	1232-18	1802	1221-60
	2000	1113-77	2000	*1208-06	2000	1209-08
TONLSD	1201	W2S3-05	2000	1101-71	2000	*1113-39
	2000	W2P2-05	2000	W2S2-05	2501	1101-71
	2501	W2P2-71	2501	W2S2-05	2501	W2S3-05
TOSCEA1	0100	*1104-11	0100	1115-64	0100	1135-29
	2700	1104-11	2700	1115-64	2700	1135-29
TPDOOA	1802	*1124-06	1802	1125-08	1802	1126-03
TPDO1A	1802	*1124-01	1802	1125-10	1802	1126-05
TPD02A	1802	*1124-09	1802	1125-04	1802	1126-08
TPD03A	1802	*1124-15	1802	1125-05	1802	1126-10
TPD04A	1802	*1124-22	1802	1125-03	1802	1126-24
TPDO5A	1802	*1124-14	1802	1125-07	1802	1126-26
TPDO6A	1802	*1124-21	1802	1125-11	1802	1126-11
TPD07A	1802	*1124-27	1802	1125-13	1802	1126-13
TPD100	1802	*1125-06	1802	1126-06		
TPD110	1802	*1125-01	1802	1126-01		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TPD120	1802	*1125-09	1802	1126-09		
TPD130	1802	*1125-15	1802	1126-22		
TPD20A	1802	1125-24	1802	*1126-04	1802	1127-03
TPD21A	1802	1125-26	1802	*1126-07	1802	1127-05
TPD22A	1802	1125-18	1802	*1126-15	1802	1127-08
TPD23A	1802	1125-20	1802	*1126-20	1802	1127-10
TPD300	1802	*1125-22	1802	1127-06		
TPD310	1802	*1125-14	1802	1127-01		
TPD40A	1802	1125-17	1802	1126-14	1802	1126-41
	1802	*1127-04				
TPD41 A	1802	1125-19	1802	1126-17	1802	1126-46
	1802	*11 27-07				
TPD500	1802	1124-68	1802	*1125-21		
TPD60A	0800	1216-10	0800	1218-54	0901	1218-37
	1802	1125-23	1802	*1126-19	1802	1213-69
TPD61A	0800	1216-05	0800	1218-56	0901	1218-38
	1802	*1124-66	1802	1125-25	1802	1213-76
TPROOA	1801	*1124-38	1801	1125-40	1801	1126-40
TPRO1 A	1801	*1124-30	1801	1125-42	1801	1126-42
TPRO2A	1801	*1124-33	1801	1125-34	1801	1126-23
TPR03A	1801	*1124-39	1801	1125-36	1801	1126-25
TPR04A	1801	*1124-52	1801	1125-29	1801	1126-35
TPRO5A	1801	*1124-46	1801	1125-31	1801	1126-37
TPR06A	1801	*1124-45	1801	1125-35	1801	1126-30
TPR07A	1801	*1124-51	1801	1125-37	1801	1126-34
TPR100	1801	*1125-38	1801	1126-21		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TPR110	1801	*1125-30	1801	1126-38		
TPR120	1801	*1125-33	1801	1126-29		
TPR130	1801	*1125-39	1801	1126-33		
TPR20A	1801	1125-54	1801	*1126-27	1801	1127-30
TPR21 A	1801	1125-56	1801	*1126-36	1801	1127-34
TPR22A	1801	1125-48	1801	*1126-31	1801	1127-40
TPR23A	1801	11 25-50	1801	*1126-39	1801	1127-42
TPR300	1801	*1125-52	1801	1127-38		
TPR310	1801	*1125-46	1801	1127-29		
TPR40A	1801	1125-41	1801	1126-52	1801	*1127-36
TPR41A	1801	1125-43	1801	1126-54	1801	*1127-31
TPR500	1801	1124-62	1801	*1125-45		
TPS500	1802	1125-68	1802	*1126-43		
TPS60A	0600	1121-35	1802	*1125-66		
TRBFBP	0800	1208-55	1201	1232-48	1201	1232-62
	1400	*1132-57	1400	1134-74		
TRBFBQ	1201	1130-47	1400	*1132-55		
TRBFRA	1400	*1130-63	1400	1132-64		
TRBFRO	1400	1130-59	1400	*1231-45		
TRCPOO	0400	*1127-20	0400	1129-01	0400	1129-10
	0400	1129-14	0400	1129-26	0400	1129-70
TRCP10	0400	*1127-19	0400	1129-30	0400	1129-42
	0400	1129-46	0400	1129-56	1400	1132-60
TRDBOO	1300	1132-08	1300	*1133-13		
TRDB10	1300	1132-05	1300	*1133-08		
TRDB20	1300	1132-24	1300	*1133-03		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TRDB30	1300	1132-18	1300	*1133-01		
TRDB40	1300	1132-40	1300	*1133-07		
TRDB50	1300	1132-34	1300	*1133-10		
TRDB60	1300	1132-54	1300	*1133-24		
TRDB70	1300	1132-48	1300	*1133-25		
TRDBEA	1400	*1133-48	1400	1136-51	2102	A10A1-R1
	2102	A1J2-21	2102	W3P2-21	2102	XA4-22
	2700	W3P1-51	2700	W3P2-21		
TRDBEAR	2102	*1134-44	2102	1136-52	2102	A10Al-Pl
	2102	AlJ2-22	2102	W3P1-52	2102	W3P2-22
	2700	W3P1-52	2700	W3P2-22		
TRDBPO	1300	1132-68	1300	*1133-18		
TRDY10	0500	1123-40	0500	1123-76	1001	*1133-56
	1001	1220-18	1202	1226-40	2000	1113-79
TRDYIB	2000	1102-71	2000	1105-76	2000	*1113-75
	2000	*1114-75	2000	W2DS1-02	2000	W2P1-71
	2501	1102-71	2501	W2DS1-02	2501	W2P1-71
TRDYIBR	0301	1102-72	0301	1106-44	2501	1102-72
	2501	W2P1-72	2501	*W2S2-04		
TRDYID	2000	1105-76	2000	*1113-75		
TRDYJD	2000	1105-76	2000	*1114-75		
TREADP	0901	*1117-11	0901	1229-57	1700	1223-04
TREADQ	0901	*1117-13	1400	1229-01	1400	1231-37
	1400	1232-14	1500	1231-01	1500	1233-01
	1500	1233-30				
TREDLA	0901	1115-11	0901	*1215-11	0901	1216-52

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TRED10	0901	*1115-13	0901	1117-08		
TRENOA	1400	*1124-72	1400	1125-74	1400	1231-48
	1400	1231-54	1500	1127-41		
TRENOR	1400	1125-65	1400	*1126-80		
TRENOS	1300	1127-54	1400	*1125-69	1400	1126-69
	1400	1133-50	1600	1226-62	1600	1226-68
TREN1A	1400	1230-18	1400	1230-31	1400	*1231-35
TREN1R	1400	1228-18	1400	*1230-23		
TREN1S	1201	1230-04	1400	*1228-14	1400	1230-14
	1400	1232-19	1500	1233-04	1500	1233-31
	1801	1233-18				
TREN2A	1400	*1222-27	1400	1228-20	1400	1228-42
TREN2R	1400	1228-40	1400	*1230-35		
TREN2S	1400	*1228-38	1400	1229-03	1400	1230-30
	1400	1231-66				
TREQ0Q	1400	*1203-25	1400	1204-24		
TREQ1Q	1400	*1204-25	1400	1205-24		
TREQ2P	1400	1126-53	1400	*1205-23		
TREQ2Q	1400	*1205-25	1400	1206-24		
TREQ3P	1400	1202-26	1400	1203-24	1400	*1206-23
TREQ3Q	1400	1126-60	1400	*1206-25		
TREQ4A	0500	1224-24	0600	1218-61	1400	*1231-59
TREQ5A	1400	*1126-55	1400	1231-43		
TREQCP	1400	*1202-23	1400	1203-22	1400	1204-22
	1400	1205-22	1400	1206-22		
TREQRA	1400	1202-22	1400	*1229-07		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TREWCA	2101	*1135-56	2101	1136-57	2101	A10A1-E3
	2101	A1J2-57	2101	W3P257	2101	XA4-29
	2101	XA4-29	2700	W3P1-57	2700	W3P2-57
TREWDP	0901	*1119-11	1802	1221-34		
TRMROA	1400	1131-80	1500	*1233-35		
TROOBQ	0400	*1129-13	0500	1123-08	1202	1134-10
TROOCA	0400	1128-15	0400	*1130-06		
TR01 BQ	0400	*1129-07	0500	1123-04	1202	1134-05
TROLCA	0400	1128-03	0400	*1130-01		
TRO2BQ	0400	*1129-25	0500	1123-03	1202	1134-07
TRO2CA	0400	1128-27	0400	*1130-09		
TR03BQ	0400	*1129-19	0500	1123-11	1202	1134-13
TR03CA	0400	1128-17	0400	*1130-15		
TRO4BQ	0400	*1129-37	0500	1123-24	1202	1134-26
TR04CA	0400	1128-39	0400	*1130-22		
TR05BQ	0400	*1129-31	0500	1123-18	1202	1134-20
TR05CA	0400	1128-29	0400	*1130-14		
TR06BQ	0400	*1129-49	0500	1113-17	1202	1134-19
TR06CA	0400	1128-51	0400	*1130-21		
TR07BQ	0400	*1129-43	0500	1113-23	1202	1134-25
TR07CA	0400	1128-41	0400	*1130-27		
TROPBQ	0400	*1129-61	1202	1134-42		
TRPC1A	1801	1125-47	1801	*1126-50		
TRPC2A	1801	*1124-60	1801	1125-49		
TRPCEO	1801	*1125-51	1801	1233-19		
TRRQOQ	1400	*1131-78	1400	1134-65		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TRRQ1A	0400	1127-14	0400	1127-22	1400	1131-79
	1400	*1134-72	1400	1230-79	1400	1231-49
TRRQ1P	1400	*1132-76	1400	1134-71	1400	1231-61
TRRQ3A	1400	1132-77	1400	*1134-69		
TRTOCA	1400	*1232-23	1802	1209-59		
TRTOCO	1400	*1130-75	1400	1132-22		
TRTDOA	0400	1125-62	1400	1131-53	1500	*1233-11
TRTDOO	0400	*1125-60	0400	1130-05	0400	1130-07
	0400	1130-08	0400	1130-13	0400	1130-19
	0400	1130-20	0400	1130-25	0400	1130-26
TRUN1 A	1002	1220-73	1002	*1223-14		
TRUN2A	1002	1220-74	1002	*1222-51		
TRUNAR	1002	*1220-76	1002	1222-76		
TRUNAS	1002	1113-65	1002	1113-76	1002	1133-64
	1002	1220-71	1002	*1222-80		
TRUNCA	1002	*1133-66	1002	1136-45	2101	A10A1-E4
	2101	A1J2-51	2101	W3P2-51	2101	XA4-33
	2700	W3P1-45	2700	W3P2-51		
TRUNCAR	1002	*1133-67	1002	1136-46	2101	A1J2-52
	2700	W3P1-46	2700	W3P2-52		
TRWC10	1400	1222-23	1700	1213-52	1700	*1223-01
	1700	1223-01	1801	1127-65	1801	1226-75
	1801	1233-14				
TRWE1A	1202	1115-33	1202	1130-73	1202	*1226-35
	1202	1231-31				
TRWE10	0500	1223-29	1202	1113-53	1202	*1115-31

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
	1202	1226-05	1202	1231-18		
TSBZYO	0500	1123-34	1001	*1218-76		
TSCI1A	1001	*1213-63	1001	1220-07		
TSNCOA	1001	1222-79	1001	*1230-76		
TSNCOR	1001	1214-65	1001	*1215-76	1001	1218-71
	1001	1224-60				
TSNCOS	1001	*1214-69	1001	1215-75	1001	1230-71
TSNC1A	1001	*1214-80	1001	1223-79		
TSNC1R	1001	1222-65	1001	1222-77	1001	*1223-75
TSNC1S	1001	1220-14	1001	*1222-75	1001	1223-65
	1001	1223-77	1202	1127-59	1202	1231-19
	1801	1127-71				
TSNC2A	1001	1222-73	1001	*1223-69	1802	1217-31
TSNC2R	1001	1221-52	1001	1222-71	1001	*1223-72
	1001	1230-72	1201	1229-17		
TSNC2S	1001	1213-57	1001	1214-76	1001	1221-75
	1001	*1222-72	1001	1223-71	1002	1220-30
	1202	1231-34				
TSNC3A	1001	*1222-69	1001	1223-73		
TSPA1A	0901	1115-62	0901	*1213-39	0901	1216-46
TSPA10	0901	*1115-60	0901	1117-24	0902	1215-50
TSPACQ	0901	*1117-25	1600	1217-37	1600	1225-53
TSPC1A	1001	1220-05	1600	*1217-35		
TSPDCA	1002	*1133-43	1002	1136-49	2101	A10A1-S4
	2101	A1J2-55	2101	W3P2-55	2101	XA4-28
	2700	W3P1-49	2700	W3P2-55		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TSPDCAR	1002	*1133-44	1002	1136-50	2101	AlJ2-56
	2700	W3P1-50	2700	W3P2-56		
TSPIOA	1002	1222-64	1002	*1227-45		
TSPI1 A	1002	1223-64	1002	*1227-51		
TSPN10	0901	*1116-09	0901	1119-24		
TSPNIR	1001	1217-18	1002	1133-45	1002	1217-50
	1002	1217-64	1002	1222-62	1002	*1223-60
	1300	1127-5,6	1600	1226-72		
TSPNIS	1001	1221-18	1002	1217-56	1002	1217-70
	1002	*1222-60	1002	1223-62	1600	1230-48
TSPNSP	0901	*1119-23	1001	1220-48	1002	1217-48
	1002	1217-62	1002	1220-34	1002	1227-47
	1802	1225-71				
TSPNSQ	0901	*1119-25	1001	1220-61	1002	1217-54
	1002	1217-68	1002	1227-41	1802	1221-62
TSTALA	2000	1115-52	2000	*1223-52		
TSTALO	2000	1114-34	2000	*1115-54		
TSTCLA	2000	1115-47	2000	*1223-46	2000	1229-06
TSTFLA	2000	1115-50	2000	1223-35	2000	*1224-31
TSTKCO	1001	1221-54	1001	*1224-51		
TSTPOR	1001	1221-46	1001	1224-45	1001	1224-79
	1001	*1225-27	1001	1226-22	1001	1229-25
	1002	1220-37	1900	1231-72	1900	1231-77
TSTPOS	1001	1224-57	1001	1225-21	1001	*1226-23
	1001	1227-17	1001	1228-26		
TSTP1A	1001	1225-23	1001	*1227-14		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TSTP1R	1001	1224-47	1001	1227-19	1001	1227-24
	1001	*1228-22	1002	1220-38		
TSTP1 S	1001	1217-14	1001	1221-14	1001	*1227-22
	1001	1228-24				
TSTP2A	1001	*1224-55	1001	1226-24		
TSTP2R	1001	1224-49	1001	1226-06	1001	*1227-09
	1002	1220-40				
TSTP2S	1001	*1226-11	1001	1227-03	1001	1227-18
	1002	1227-43	1002	1227-49	1002	1227-64
	1002	1227-70				
TSTP4A	1001	*1221-76	1001	1226-25		
TSTP6A	1001	*1224-63	1001	1225-46	1001	1227-26
	1002	1220-72				
TSTP8A	1001	*1217-21	1001	1226-08	2000	1221-38
TSTP9A	1001	*1221-21	1001	1226-10		
TSTPRA	0200	1212-30	1001	*1227-21		
TSTROA	1001	*1221-47	1001	1223-61		
TSTROR	1001	1223-59	1001	*1224-64		
TSTROS	1001	1221-43	1001	*1223-63	1001	1224-66
	1001	1224-77	1001	1229-21		
TSTR1A	1001	1224-68	1001	*1227-46		
TSTR1R	1001	1223-76	1001	*1224-73	1001	1229-23
TSTR1S	1001	1220-43	1001	1220-55	1001	1222-43
	1001	*1223-80	1001	1224-75	1001	1228-56
TSTR2A	1001	*1221-45	1001	1223-78	1001	1227-07
	1002	1227-78				

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TSTR2R	1001	*1225-43	1001	1226-49		
TSTR2S	1001	1225-41	1001	*1226-47	1001	1227-48
	1600	1230-46	1802	1221-55	1802	1225-65
TSTR3A	1001	*1222-45	1001	1227-56		
TSTR3R	1001	1220-46	1001	1220-60	1001	1227-54
	1001	*1228-52				
TSTR3S	1001	1221-71	1001	*1227-52	1001	1228-54
TSTR4A	1001	*1221-69	1001	1226-43	1001	1226-52
TSTR6A	1001	*1220-47	1001	1226-46	1001	1226-54
TSTR8A	1001	*1220-59	1001	1226-48	1001	1226-56
TSTR90	1001	*1226-45	1201	1134-79	1201	1223-10
	1400	1124-73	1400	1222-25		
TSTRLA	2000	1221-40	2000	*1224-36	2000	1229-08
TSTRRA	0200	1212-31	1001	*1229-27		
TSTTLA	2000	1223-37	2000	*1224-39	2000	1229-10
TSYN10	0901	*1216-47	0901	1218-40		
TTCPOO	1300	1132-01	1300	1132-10	1300	1132-14
	1300	1132-26	1300	1132-70	1300	*1133-54
	1600	1230-50				
TTCP10	1300	1132-30	1300	1132-42	1300	1132-46
	1300	1132-56	1300	*1133-49		
TTMERD1	1802	*1114-39	1802	1135-48		
TTMERP	1201	1232-34	1400	1230-22	1400	1231-68
	1802	*1207-76	1802	1217-77		
TTMERQ	0500	1123-65	1802	1114-35	1802	*1207-78
TTMESA	1802	1207-80	1802	*1208-63		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TTMESO	1802	1208-59	1802	*1209-63		
TTOOBP	1300	*1132-11	1500	1233-43	1801	1124-34
TTOOBQ	0400	1130-10	1300	*1132-13	1801	1124-40
	1801	1131-10				
TTO1BP	1300	*1132-09	1500	1233-46	1801	1124-36
TTO1BQ	0400	1130-04	1300	*1132-07	1801	1124-42
	1801	1131-01				
TTO2BP	1300	*1132-23	1500	1233-48	1801	1124-35
TTO2BQ	0400	1130-03	1300	*1132-25	1801	1124-29
	1801	1131-26				
TT03BP	1300	*1132-21	1500	1233-49	1801	1134-37
TTO3BQ	0400	1130-11	1300	*1132-19	1801	1124-31
	1801	1131-14				
TT04BP	1300	*1132-35	1500	1233-50	1801	1124-48
TT04BQ	0400	1130-24	1300	*1132-37	1801	1124-54
	1801	1131-42				
TT05BP	1300	*1132-33	1500	1233-52	1801	1124-50
TTO5BQ	0400	1130-18	1300	*1132-31	1801	1124-56
	1801	1131-30				
TT06BP	1300	*1132-47	1500	1233-54	1801	1124-47
TT06BQ	0400	1130-17	1300	*1132-49	1801	1124-41
	1801	1131-56				
TT07BP	1300	*1132-45	1500	1233-56	1801	1124-49
TT07BQ	0400	1130-23	1300	*1132-43	1801	1124-43
	1801	1131-46				
TTOPBP	1300	*1132-59	1500	1134-76	1801	1126-56

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TTOPBQ	1300	*1132-61	1801	1124-64	1801	1131-70
TTPERO	0500	1123-68	1802	*1214-63		
TTRSOA	1300	1132-04	1300	1132-06	1300	1132-20
	1300	1132-22	1300	1132-66	1300	*1133-78
TTRSOO	1300	*1127-50	1300	1133-75	1300	1133-76
TTRS1A	1300	1132-36	1300	1132-38	1300	1132-50
	1300	1132-52	1300	*1133-77		
TTRSCA	1300	1127-52	1500	*1126-63		
TWDBOA	1202	*1134-06	1202	1136-63	2200	A10A1-K1
	2200	A1J2-27	2200	A1J2-27	2200	XA1-12
	2700	W3P1-63	2700	W3P2-27		
TWDBOAR	1202	*1134-02	1202	1136-64	2200	A10A1-L3
	2200	A1 J2-28	2700	W3P1-64	2700	W3P2-28
TWDB1A	1202	*1134-01	1202	1136-65	2200	A10A1-L1
	2200	A1J2-29	2200	A1J2-29	2200	XA2-11
	2700	W3P1-65	2700	W3P2-29		
TWDB1AR	1202	*1134-02	1202	1136-66	2200	A10A1-L2
	2200	A1J2-30	2700	W3P1-66	2700	W3P2-30
TWDB2A	1202	*1134-09	1202	1136-69	2200	A10A1-M7
	2200	A1J2-31	2200	AlJ2-31	2200	XA2-10
	2700	W3P1-69	2700	W3P2-31		
TWDB2AR	1202	*1134-02	1202	1136-70	2200	A10A1-L6
	2200	A1 J2-32	2700	W3P1-70	2700	W3P2-32
TWDB3A	1202	*1134-15	1202	1136-71	2200	A10A1-M4
	2200	A1J2-33	2200	A1J2-33	2200	XA3-11
	2700	W3P1-71	2700	W3P2-33		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TWDB3AR	1202	*1134-16	1202	1136-72	2200	A10A1-M3
	2200	A1J2-34	2700	W3P1-72	2700	W3P2-34
TWDB4A	1202	*1134-22	1202	1136-73	2200	A10A1-K3
	2200	A1J2-35	2200	A1J2-35	2200	XA1-11
	2700	W3P1-73	2700	W3P2-35		
TWDB4AR	1202	*1134-16	1202	1136-74	2200	A10A1-L5
	2200	A1J2-36	2700	W3P1-74	2700	W3P2-36
TWDB5A	1202	*1134-14	1202	1136-75	2200	A10A1-N1
	2200	A1J2-37	2200	A1J2-37	2200	XA3-12
	2700	W3P1-75	2700	W3P2-37		
TWDB5AR	1202	*1134-16	1202	1136-76	2200	A10A1-N2
	2200	A1J2-38	2700	W3P1-76	2700	W3P2-38
TWDB6A	1202	*1134-21	1202	1136-77	2200	A10A1-K2
	2200	A1J2-39	2200	A1J2-39	2200	XA1-10
	2700	W3P1-77	2700	W3P2-39		
TWDB6AR	1202	*1134-32	1202	1136-78	2200	A10A1-L4
	2200	A1J2-40	2700	W3P1-78	2700	W3P2-40
TWDB7A	1202	*1134-27	1202	1136-79	2200	A10A1-M5
	2200	A1J2-41	2200	A1J2-41	2200	XA3-10
	2700	W3P1-79	2700	W3P2-41		
TWDB7AR	1202	*1134-32	1202	1136-80	2200	A10A1-M6
	2200	A1J2-42	2700	W3P1-80	2700	W3P2-42
TWDBEA	1202	1104-10	1202	*1133-46	2700	1104-10
	2700	1133-46				
TWDBEB	1202	*1104-09	1202	1136-53	2102	1104-9
	2102	A10A1-N8	2102	A1J2-47	2102	W3P1-53

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
	2102	W3P2-47	2102	W3P2-47	2102	XA4-25
	2700	1104-09	2700	1136-53		
TWDBPA	1202	*1134-38	1202	1136-61	2200	A10A1-M1
	2200	A1J2-25	2200	A1J2-25	2200	XA2-12
	2700	W3P1-61	2700	W3P2-25		
TWDBPAR	1202	*1134-44	1202	1136-62	2200	A10A1-M2
	2200	A1J2-26	2700	W3P1-62	2700	W3P2-26
TWDBSA	1202	*1134-30	1202	1136-59	2200	A10A1-N4
	2200	A1J2-43	2200	A1J2-43	2200	XA3-08
	2700	W3P1-59	2700	W3P2-43		
TWDBSAR	1202	*1134-32	1202	1136-60	2200	A10A1-N3
	2200	A1J2-44	2700	W3P1-60	2700	W3P2-44
TWENOA	1202	1227-13	1202	*1231-21		
TWENOR	1202	*1226-09	1202	1227-11		
TWENOS	1201	1229-14	1202	1133-41	1202	1226-01
	1202	*1227-15				
TWEN1 A	1202	*1127-63	1202	1226-04		
TWENA04	1201	1101-39	1201	*W2S3-01	1202	1105-38
	1202	1226-38	2501	1101-39	2501	W2P2-39
	2501	*W2S3-01				
TWENAOR	2501	1101-40	2501	1105-32	2501	W2P2-40
	2501	*W2S3-06				
TWENCA	1202	*1124-63	1202	1127-57		
TWENCO	1202	1124-59	1202	*1127-55	1202	1130-71
	1202	1231-14	1202	1231-30		
TWENIB	1202	1102-73	1202	*1113-57	1202	*1114-57

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
	1202	W2S3-08	2501	1102-73	2501	W2P1-73
	2501	W2S3-08				
TWENIBR	0301	1102-74	0301	1106-44	2501	1102-74
	2501	W2P1-74	2501	*W2S3-04		
TWENID	1202	1102-73	1202	*1113-57		
TWENJD	1202	1102-73	1202	*1114-57		
TWENSD	1802	1101-74	1802	*1113-45	1802	W2P2-74
	1802	W2S5-05	2501	1101-74	2501	W2P2-74
	2501	W2S5-05				
TWLRCA	1201	*1134-33	1201	1136-55	1201	A1J2-45
	2102	A10A1-N5	2102	A1J2-45	2102	W3P2-45
	2102	XA4-24	2700	W3P1-55	2700	W3P2-45
TWLRCAR	1201	*1134-58	1201	1136-56	1201	A1J2-46
	2102	A10A1-N6	2102	A1J2-46	2700	W3P1-56
	2700	W3P2-46				
TWLRCO	1201	1134-29	1201	*1229-19		
TWPEOA	1201	*1134-63	1201	1226-34	1201	1230-06
TWPEOO	1201	*1130-52	1201	1134-61		
TWRDOQ	0800	*1128-78	0800	1208-53		
TWRD1A	0400	1127-17	0400	1127-24	0800	1128-79
	0800	*1208-60	1201	1130-49	1201	1202-04
	1400	1231-52				
TWRD1P	0800	*1129-76	0800	1208-62		
TWRD3A	0800	1129-77	0800	*1208-57		
TWRGOA	1201	1222-13	1201	*1223-06		
TWRGOO	1201	*1130-66	1201	1223-08		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TWRGOR	1201	*1221-09	1201	1222-11		
TWRGOS	1201	1125-55	1201	1127-33	1201	1130-35
	1201	1221-01	1201	*1222-15		
TWRG1A	1201	*1130-60	1201	1221-04		
TWRG1R	1201	1124-53	1201	*1125-57	1201	1130-29
	1201	1130-37				
TWRG1S	1201	*1124-57	1201	1125-53	1201	1127-09
	1201	1226-18				
TWRG2A	1201	1124-55	1201	*1127-39		
TWRG2R	1201	1126-45	1201	*1127-51	1201	1232-60
TWRG2S	0901	1221-24	1201	*1126-51	1201	1127-45
	1201	1130-62				
TWRG3A	1201	1127-47	1201	*1130-33		
TWRG4A	1201	1126-49	1201	*1127-15		
TWRG6A	1201	1126-47	1201	*1226-21	1201	1228-10
TWRGRA	0200	1212-38	1201	*1130-39		
TWRIOR	1201	1228-08	1201	*1230-11	1201	1232-49
TWRIOS	1201	*1228-06	1201	1230-01	1202	1224-78
	1202	1231-55	1802	1225-75		
TWRI1A	1201	1230-05	1201	*1232-59		
TWRI1R	1201	1232-64	1202	*1224-80	1202	1225-69
TWRI1S	1202	1134-53	1202	1224-69	1202	*1225-80
	1202	1228-36	1202	1229-29		
TWRI2A	1202	1225-76	1202	*1231-57		
TWRI2R	1202	1134-55	1202	1134-62	1202	1227-34
	1202	*1228-30	1202	1231-60		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TWRI2S	1100	1211-61	1201	1232-06	1202	1134-34
	1202	*1227-30	1202	1228-34	1202	1229-33
TWRI3A	1202	*1134-66	1202	1224-76	1400	1231-46
TWRI3R	1202	1228-29	1202	*1229-36	1202	1231-62
TWRI3S	1202	1134-68	1202	*1228-33	1202	1229-38
TWRI4A	1202	1227-36	1202	*1229-31		
TWRI5A	1202	*1134-60	1202	1229-40		
TWRI6A	1202	1228-31	1202	*1229-39		
TWRIRA	1100	1213-66	1202	*1134-57		
TWRITP	0901	*1117-09	0901	1229-59	1201	1130-68
	1202	1127-53	1700	1223-05		
TWRITQ	0800	1216-30	0901	*1117-07	1201	1134-59
	1201	1134-77	1201	1226-14	1201	1231-22
	1201	1232-01	1201	1232-30	1802	1216-55
TWRQOA	0600	1218-55	1201	*1232-35		
TWRQOQ	1201	*1203-07	1201	1204-05		
TWRQ1A	0600	1218-60	1201	*1134-75		
TWRQ1Q	1201	*1204-07	1201	1205-05		
TWRQ2P	1201	*1205-09	1201	1232-36		
TWRQ2Q	1201	*1205-07	1201	1206-05		
TWRQ3P	1201	1202-01	1201	1203-05	1201	*1206-09
TWRQ3Q	1201	*1206-07	1201	1232-37		
TWRQCP	1201	*1202-09	1201	1203-04	1201	1204-04
	1201	1205-04	1201	1206-04		
TWRT1A	0901	1115-04	0901	1216-54	0901	*1217-09
TWRT10	0901	*1115-03	0901	1117-05		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TWTOCA	1201	*1232-11	1802	1209-61		
TWTOCO	1201	*1130-51	1201	1232-07		
TX1MAP	0100	*1206-57	0100	1208-65		
TX1MAQ	0100	*1206-55	0100	1207-62	0100	1208-76
TX1MBP	0100	1206-62	0100	*1207-57	0100	1208-78
TX1MBQ	0100	*1207-55	0100	1208-74		
TXAOCB4	0302	1105-08	0302	*1113-06	0302	*1114-06
	0302	1122-15				
TXAOCD	0302	1105-08	0302	*1113-06		
TXAOCG	0302	1101-14	0302	1108-40	0302	W2J1-D
	2502	1101-14	2502	W2J1-D	2502	W2P2-14
TXAOCH	0302	1101-13	0302	1108-38	0302	W2J1-C
	2502	1101-13	2502	W2J1-C	2502	W2P2-13
TXAOCT	0302	*1108-07	0302	1113-10		
TXA1CD4	0302	1105-10	0302	*1113-01	0302	1122-03
TXA1CG	0302	1101-18	0302	1108-36	0302	W2J1-F
	2502	1101-18	2502	W2J1-F	2502	W2P2-18
TXA1CH	0302	1101-17	0302	1108-34	0302	W2J1-E
	2502	1101-17	2502	W2J1-E	2502	W2P2-17
TXA1CT	0302	*1108-11	0302	1113-05		
TXA2CD4	0302	1105-05	0302	*1113-09	0302	1122-27
TXA2CG	0302	1101-20	0302	1109-40	0302	W2J1-H
	2502	1101-20	2502	W2J1-H	2502	W2PW2-20
TXA2CH	0302	1101-19	0302	1109-38	0302	W2J1-G
	2502	1101-19	2502	W2J1-G	2502	W2P2-19
TXA2CT	0302	*1109-07	0302	1113-07		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TXA3CB4	0302	1105-07	0302	*1113-15	0302	*1114-15
	0302	1122-17				
TXA3CD	0302	1105-07	0302	*1113-15		
TXA3CG	0302	1101-22	0302	1109-36	0302	W2J1-K
	2502	1101-22	2502	W2J1-K	2502	W2P2-22
TXA3CH	0302	1101-21	0302	1109-34	0302	W2J1-J
	2502	1101-21	2502	W2J1-J	2502	W2P2-21
TXA3CT	0302	*1109-11	0302	1113-13		
TXA4CB4	0302	1105-09	0302	*1113-22	0302	*1114-22
	0302	1122-39				
TXA4CD	0302	1105-09	0302	*1113-22		
TXA4CG	0302	1101-23	0302	1110-40	0302	W2J1-M
	2502	1101-24	2502	W2J1-M	2502	W2P2-24
TXA4CH	0302	1101-24	0302	1110-38	0302	W2J1-L
	2502	1101-23	2502	W2J1-L	2502	W2P2-23
TXA4CT	0302	*1110-07	0302	1113-26		
TXA5CB4	0302	1105-20	0302	*1113-14	0302	*1114-14
	0302	1122-29				
TXA5CD	0302	1105-20	0302	*1113-14		
TXA5CG	0302	1101-26	0302	1110-36	0302	W2J1-P
	2502	1101-26	2502	W2J1-P	2502	W2P2-26
TXA5CH	0302	1101-25	0302	1110-34	0302	W2J1-N
	2502	1101-25	2502	W2J1-N	2502	W2P2-25
TXA5CT	0302	*1110-11	0302	1113-20		
TXA6CD4	0302	1105-26	0302	*1113-21	0302	1122-51
TXA6CG	0302	1101-30	0302	1111-40	0302	W2J1-S

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
	2502	1101-30	2502	W2J1-S	2502	W2P2-30
TXA6CH	0302	1101-29	0302	1111-38	0302	W2J1-R
	2502	1101-29	2502	W2J1-R	2502	W2P2-29
TXA6CT	0302	*1111-07	0302	1113-19		
TXA7CB4	0302	1105-24	0302	*1113-27	0302	*1114-27
	0302	1122-41				
TXA7CD	0302	1105-24	0302	*1113-27		
TXA7CG	0302	1101-34	0302	1111-36	0302	W2J1-U
	2502	1101-34	2502	W2J1-U	2502	W2P2-34
TXA7CH	0302	1101-33	0302	1111-34	0302	W2J1-T
	2502	1101-33	2502	W2J1-T	2502	W2P2-33
TXA7CT	0302	*1111-11	0302	1113-25		
TXACMB4	0301	1105-19	0301	*1113-30	0301	*1114-30
	0301	1122-53				
TXACMD	0301	1105-19	0301	*1113-30		
TXACMG	0301	1101-06	0301	1107-40	0301	*W2J1-g
	2502	1101-06	2502	W2J1-q	2502	W2P2-06
TXACMH	0301	1101-05	0301	1107-38	0301	*W2J1-p
	2502	1101-05	2502	W2J1-p	2502	W2P2-05
TXACMT	0301	*1107-07	0301	1113-36	0301	1213-38
TXADOA	0800	*1116-66	0800	1212-14		
TXAD1A	0800	*1116-60	0800	1212-18		
TXAD2A	0800	*1116-57	0800	1212-19		
TXAD3A	0800	*1116-63	0800	1212-20		
TXAD4A	0800	*1116-75	0800	1212-22		
TXAD5A	0800	*1116-72	0800	1212-24		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TXAD6A	0800	*1116-69	0800	1212-25		
TXAD7A	0800	*1116-80	0800	1212-26		
TXADRO	0800	*1212-23	0800	1216-01	0800	1218-43
TXAEND4	0301	1105-36	0301	*1113-33	0301	1122-80
TXAENG	0301	1101-08	0301	1107-36	0301	*W2J1-n
	2502	1101-08	2502	*W2J1-n	2502	W2P2-08
TXAENH	0301	1101-07	0301	1107-34	0301	*W2J 1-m
	2502	1101-07	2502	*W2J1-m	2502	W2P2-07
TXAENT	0301	*1107-11	0301	1113-31	0301	1213-40
TXAIEA	0301	1115-35	0301	1115-38	0500	*1211-09
TXAIEO	0301	*1115-40	0302	1113-03	0302	1113-04
	0302	1113-08	0302	1113-11	0302	1113-17
	0302	1113-18	0302	1113-23	0302	1113-24
TXAIFO	0301	1113-29	0301	1113-34	0301	1113-40
	0301	*1115-37				
TXAING	0301	1101-36	0301	1106-36	0301	*W2J1-s
	2502	1101-36	2502	*W2J1-s	2502	W2P2-36
TXAINH	0301	1101-35	0301	1106-34	0301	*W2J1-r
	2502	1101-35	2502	*W2J1-r	2502	W2P2-35
TXAPCB4	0301	*1113-38	0301	*1113-38	0301	*1114-38
	0301	1122-63				
TXAPCD	0301	1105-17	0301	1113-38		
TXAPCG	0301	1101-10	0301	1112-40	0301	W2J1-B
	2502	1101-10	2502	W2J1-B	2502	W2P2-10
TXAPCH	0301	1101-09	0301	1112-38	0301	W2J1-A
	2502	1101-09	2502	W2J1-A	2502	W2P2-09

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TXAPCT	0301	*1112-07	0301	1113-42		
TXARQA	0301	1106-03	0600	1128-53	0600	*1213-51
TXARQG	0301	1101-04	0301	1106-40	0301	*W2S9C-C
	2502	1101-04	2502	W2P2-04	2502	*W2S9C-C
TXARQH	0301	1101-03	0301	1106-38	0301	*W2S9B-C
	2502	1101-03	2502	W2P2-03	2502	*W2S9B-C
TXARSA	0301	*1213-36	0700	1224-08		
TXASOA4	0800	1101-49	0800	1105-47	0800	1214-04
	0800	*W2S9A-01	2502	1101-49	2502	W2P2-49
	2502	*W2S9A-01				
TXASOAR	0800	*1101-50	0800	1105-44		
TXASOO	0800	1116-70	0800	*1214-01		
TXAS10	0800	*1115-68	0800	1116-64		
TXAS1A4	0800	1101-51	0800	1105-45	0800	1115-65
	0800	*W2S9A-02	2502	1101-51	2502	W2P2-51
	2502	*W2S9A-02				
TXAS1AR	0800	*1101-52	0800	1105-44		
TXAS2A4	0800	1101-53	0800	1105-41	0800	1115-79
	0800	*W2S9A-03	2502	1101-53	2502	W2P2-53
	2502	*W2S9A-03				
TXAS2AR	0800	*1101-54	0800	1105-32		
TXAS20	0800	*1115-80	0800	1116-55		
TXAS3A4	0800	1101-55	0800	1105-62	0800	1115-73
	0800	*W2S9A-04	2502	1101-55	2502	W2P2-55
	2502	*W2S9A-04				
TXAS3AR	0800	*1101-56	0800	1105-67		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TXAS30	0800	*1115-71	0800	1116-61		
TXAS4A4	0800	1101-59	0800	1105-56	0800	1115-69
	0800	*W2S9A-05	2502	1101-59	2502	WZPZ-59
	2502	*W2S9A-05				
TXAS4AR	0800	*1101-60	0800	1105-67		
TXAS40	0800	*1115-70	0800	1116-79		
TXAS5A4	0800	1101-61	0800	1105-55	0800	1115-74
	0800	*W2S9A-06	2502	1101-61	2502	W2P2-61
	2502	*W2S9A-06				
TXAS5AR	0301	*1101-62	0301	1106-58		
TXAS50	0800	*1115-72	0800	1116-73		
TXAS6A4	0800	1101-63	0800	1105-53	0800	1115-76
	0800	*W2S9A-07	2502	1101-63	2502	W2P2-63
	2502	*W2S9A-07				
TXAS6AR	0301	*1101-64	0301	1106-58		
TXAS60	0800	*1115-78	0800	1116-74		
TXAS7A4	0800	1101-65	0800	1105-51	0800	1115-75
	0800	*W2S9A-08	2502	1101-65	2502	W2P2-65
	2502	*W2S9A-08				
TXAS7AR	0301	*1101-66	0301	1106-44		
TXAS70	0800	*1115-77	0800	1116-78		
TXBOCD	0302	1105-08	2000	*1114-06		
TXB3CD	0302	1105-07	2000	*1114-15		
TXB4CD	0302	1105-09	2000	*1114-22		
TXB5CD	0302	1105-20	2000	*1114-14		
TXB7CD	0302	1105-24	2000	*1114-27		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TXBCMD	0301	1105-19	2000	*1114-30		
TXBPCD	0301	1105-17	2000	*1114-38		
TXCAOA	0800	1214-42	0800	*1216-11		
TXCA1 A	0901	1214-29	0901	*1216-23		
TXCA10	0901	*1214-33	0901	1215-22	0901	1218-01
	0902	1215-43	0902	1216-71	0902	1218-14
TXCK10	0100	*1209-38				
TXCK30	0100	*1209-66				
TXCL10	0100	*1209-30				
TXCL30	0100	*1209-60				
TXCM10	0100	*1209-33				
TXCM30	0100	*1209-57				
TXCMAR	0800	1214-40	0800	*1215-35		
TXCMAS	0800	1213-30	0800	*1214-38	0800	1215-37
	0901	1216-14				
TXCN10	0100	*1209-39				
TXCP1A	0100	*1208-69	0100	1209-29	0100	1209-34
	0100	1209-35	0100	1209-40	0100	1209-41
	0100	1209-47	0100	1209-48		
TXCP1B	0100	*1209-30	0100	*1209-33	0100	*1209-38
	0100	*1209-39	1001	1217-20	1001	1220-24
	1001	1220-50	1001	1220-64	1001	1221-20
	1001	1221-50	1001	1221-74	1001	1222-20
	1001	1223-74	1001	1224-05	1001	1224-61
	1001	1225-13	1001	1227-74	1002	1225-56
	1002	1225-61	1201	1203-01	1201	1204-01

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
	1201	1205-01	1201	1206-01	1201	1225-49
	1201	1226-20	1201	1229-49	1202	1229-34
	1202	1229-37	1400	1203-26	1400	1204-26
	1400	1205-26	1400	1206-26		
TXCP10	0100	*1209-46				
TXCP3A	0100	*1208-80	0100	1209-53	0100	1209-62
	0100	1209-65	0100	1209-68	0100	1209-71
	0100	1209-76	0200	1209-17	1100	1210-76
TXCP3B	0100	*1209-57	0100	*1209-60	0100	*1209-66
	0800	1208-64	0901	1213-62	1001	1213-61
	1001	1213-72	1001	1213-79	1001	1214-78
	1001	1221-56	1001	1224-62	1001	1227-10
	1001	1227-20	1001	1227-50	1002	1220-42
	1201	1232-10	1500	1231-07	1500	1231-13
	1500	1233-07	1600	1217-42	1600	1225-62
	1600	1227-25	1600	1228-07	1600	1228-37
	1700	1213-56	1801	1233-24	1802	1221-36
	1900	1222-37	1900	1222-56	1900	1227-31
	1900	1227-37				
TXCP30	0100	*1209-72				
TXCQ1B	0100	*1209-45	0100	*1209-46	0100	*1209-51
	0800	1129-79	0901	1118-46	0902	1119-46
	0902	1119-60	1002	1228-64	1201	1127-13
	1201	1127-37	1201	1130-31	1201	1134-50
	1201	1232-66	1202	1127-61	1202	1134-64
	1202	1231-20	1400	1132-79	1500	1131-72

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
	1500	1132-72	1600	1127-70	1600	1130-43
	1600	1225-70	1600	1226-74	1801	1127-72
	1900	1223-61	1900	1227-42	1900	1229-72
	1900	1229-79				
TXCQ10	0100	*1209-45				
TXCQ3B	0100	*1209-69	0100	*1209-72	0100	*1209-80
	0901	1116-31	0901	1221-26	0902	1116-37
	0902	1116-42	1001	1130-75	1001	1221-79
	1002	1228-70	1201	1130-64	1201	1134-56
	1201	1231-26	1201	1232-38	1201	1232-50
	1202	1134-70	1202	1231-36	1202	1231-64
	1400	1126-62	1400	1134-73	1400	1231-42
	1400	1231-70	1400	1232-24	1500	1126-61
	1500	1127-78	1500	1233-37	1600	1124-79
	1600	1134-49	1600	1225-10	1600	1230-52
	1801	1226-79	1900	1231-74	1900	1231-79
TXCQ30	0100	*1209-69				
TXCR10	0100	*1209-51				
TXCR30	0100	*1209-80				
TXDB00	0302	1122-08	0500	*1121-43		
TXDB10	0302	1122-05	0500	*1121-51		
TXDB20	0302	1122-24	0500	*1121-64		
TXDB30	0302	1122-18	0500	*1121-55		
TXDB40	0302	1122-40	0500	*1121-63		
TXDB50	0302	1122-34	0500	*1121-73		
TXDB60	0302	1122-54	0500	*1121-74		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TXDB70	0302	1122-48	0500	*1121-80		
TXDD0A	0500	1121-41	0500	*1123-06		
TXDD1A	0500	1121-45	0500	*1123-01		
TXDD2A	0500	1121-66	0500	*1123-09		
TXDD3A	0500	1121-53	0500	*1123-15		
TXDD4A	0500	1121-57	0500	*1123-22		
TXDD5A	0500	1121-75	0500	*1123-14		
TXDD6A	0500	*1113-21	0500	1121-65		
TXDD7A	0500	*1113-27	0500	1121-69		
TXDDCA	0302	1121-54	0500	1116-11	0500	*1209-52
TXDDC0	0500	1113-19	0500	1113-25	0500	*1116-15
	0500	1123-05	0500	1123-07	0500	1123-10
	0500	1123-13	0500	1123-20	0500	1123-26
TXDEVR	0901	1208-24	0901	*1209-22	1700	1116-05
	1700	1116-10	1700	1124-74		
TXDEVS	0901	*1208-22	0901	1209-24	0901	1214-68
	0901	1218-30				
TXDI0A	0500	1121-48	0500	*1123-66		
TXDI1A	0500	1121-49	0500	*1123-60		
TXDI2A	0500	1121-70	0500	*1123-57		
TXDI3A	0500	1121-62	0500	*1123-63		
TXDI4A	0500	1121-61	0500	*1123-75		
TXDI5A	0500	1121-79	0500	*1123-72		
TXDI6A	0500	1121-72	0500	*1123-69		
TXD00A	0302	1108-03	0302	*1121-04		
TXD01A	0302	1108-10	0302	*1121-07		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TXD02A	0302	1109-03	0302	*1121-15		
TXD03A	0302	1109-10	0302	*1121-20		
TXD04A	0302	1110-03	0302	*1121-19		
TXD05A	0302	1110-10	0302	*1121-27		
TXD06A	0302	1111-03	0302	*1121-36		
TXD07A	0302	1111-10	0302	*1121-31		
TXD0IA	0301	1106-10	0302	*1121-50		
TXD0PA	0301	1112-03	0600	*1121-39		
TXDPEA	1201	1226-36	1201	1230-07	1802	*1216-59
TXDS0A	0500	1121-46	0500	*1123-38		
TXDS1A	0500	1121-47	0500	*1123-30		
TXDS2A	0500	1121-68	0500	*1123-33		
TXDS3A	0500	1121-60	0500	*1123-39		
TXDS5A	0500	1121-77	0500	*1123-46		
TXDS6A	0500	1121-71	0500	*1123-45		
TXDV0A	0901	1208-26	0901	*1215-23		
TXDV1A	0600	1209-77	0901	1214-48	0901	1214-54
	0901	*1218-35	1001	1214-74		
TXDV1B	0901	1117-01	0901	1117-10	0901	1117-26
	0901	1118-01	0901	1118-10	0901	1118-26
	0901	1119-01	0901	1119-10	0901	1119-26
	0901	*1214-46	0901	*1214-52	1700	1116-19
	1700	1116-20	1700	1116-25	1700	1116-26
TXDV10	0901	*1214-52				
TXDV20	0901	*1214-46				
TXDVCA	0901	1115-61	0901	1116-03	0901	*1215-09

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
	0901	1216-43				
TXDVC0	0901	*1115-63	0901	1119-08	0901	1215-25
TXEA0A	0600	1128-60	0800	1209-11	0800	1214-36
	0800	*1218-47				
TXEA00	0500	1208-07	0500	1208-11	0800	*1209-15
	1400	1229-05				
TXEA1A	0800	*1115-34	0800	1215-36		
TXEA10	0800	1115-36	0800	*1208-21		
TXEB0A	0902	1117-53	0902	*1216-76		
TXEB0Q	0902	*1117-55	0902	1119-62		
TXEB1A	0902	*1116-38	0902	1117-60		
TXEB1Q	0901	1213-60	0902	1116-40	0902	*1119-55
	1201	1231-24	1400	1231-38	1700	1213-54
TXED0A	0400	1130-34	0400	1130-40	0800	1128-80
	0800	*1216-35				
TXENAR	0800	1214-34	0800	*1215-33		
TXENAS	0800	*1214-30	0800	1215-30	0800	1216-31
	1802	1216-60				
TXGN1A	0100	*1115-66	0100	1120-50	0500	1207-05
	0500	1207-18	0500	1207-24	0600	1122-71
	0600	1128-62	0600	1207-08	0800	1128-77
	0901	1117-54	0902	1117-48	0902	1117-62
	1400	1131-77				
TXHS0A	0902	1117-41	0902	*1215-45		
TXIN0A	0800	*1213-31	0800	1214-13		
TXINHR	0500	1225-17	0600	1213-05	0600	1213-47

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
	0800	1208-19	0800	1213-09	0800	*1214-15
	1500	1233-42				
TXINHS	0800	*1213-15	0800	1214-11		
TXIR0A	0500	1207-17	0902	*1218-23		
TX0D0A	0400	1130-36	0400	1130-42	0600	1209-79
	0901	1117-51	0901	*1215-09		
TX0DRA	0400	1127-23	0901	1117-04	0901	*1209-09
	1802	1217-34				
TX0FRR	0901	1208-18	0901	*1209-14		
TX0FR$	0901	*1208-14	0901	1209-08	0901	1209-18
	0901	1215-49				
TX0R0A	0901	1208-20	0901	*1218-11		
TXR0P0	1802	*1125-27	1802	1216-61		
TXRS0A	0700	*1210-13				
TXRS0B	0200	1212-42	0301	1213-10	0500	1207-04
	0500	1207-20	0500	1207-22	0500	1225-26
	0600	1207-06	0700	*1210-01	0700	*1210-03
	0700	*1210-08	0700	*1210-13	0800	1213-11
	0800	1213-29	0800	1215-42	1001	1224-25
	1001	1225-25	1001	1225-48	1001	1226-13
	1001	1229-13	1002	1224-48	1201	1202-03
	1201	1225-37	1201	1229-26	1201	1230-08
	1202	1226-07	1202	1229-42	1400	1202-27
	1400	1230-25	1400	1230-37	1600	1229-48
	1600	1229-56	1802	1217-36	2000	1221-42
	2000	1222-48				

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TXRS00	0700	1210-04	0700	1210-05	0700	1210-06
	0700	1210-11	0700	1210-17	0700	1210-20
	0700	1210-22	0700	1210-23	0700	1214-41
	0700	1214-47	0700	*1224-04		
TXRS1A	0700	*1210-08				
TXRS1B	0400	1127-25	0600	1128-64	0700	*1210-14
	0700	*1210-18	0700	*1210-24	0700	*1210-25
	0800	1128-75	0800	1129-80	0901	1117-06
	0901	1117-22	0901	1118-22	0901	1119-22
	1001	1125-05	1001	1215-79	1001	1221-13
	1002	1220-75	1100	1213-70	1201	1126-70
	1201	1127-49	1201	1221-07	1400	1126-78
	1400	1131-75	1400	1132-80	1400	1231-50
	1400	1231-56	1500	1127-48	1500	1129-65
	1600	1126-72	1600	1126-79	1600	1226-64
	1600	1226-70				
TXRS2A	0700	*1210-03				
TXRS2B	0600	1122-73	0700	1117-65	0700	1118-80
	0700	*1214-45	0700	*1214-51	0901	1117-52
	0901	1118-04	0901	1118-06	0901	1118-50
	0901	1119-04	0901	1119-06	0902	1117-64
	0902	1119-64				
TXRS3A	0700	*1210-01				
TXRS4A	0700	*1210-24				
TXRS5A	0700	*1210-25				
TXRS6A	0700	*1210-18				

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TXRS7A	0700	*1210-14				
TXRS8A	0700	*1214-45				
TXRS9A	0700	*1214-51				
TXS0BP	0302	*1122-11	0302	1212-01	1802	1124-04
TXS0BQ	0302	1121-08	0302	*1122-13	0400	1128-08
	0800	1116-68	0901	1216-24	1700	1116-24
	1802	11 24-08				
TXS1BP	0302	*1122-09	0302	1212-04	0901	1216-25
	1802	11 24-05				
TXS1BQ	0302	1121-03	0302	*1122-07	0400	1128-05
	0800	1116-62	1700	1116-18	1802	1124-10
TXS2BP	0302	*1122-23	0302	1212-05	0901	1216-26
	1802	1124-11				
TXS2BQ	0302	1121-11	0302	*1122-25	0400	1128-24
	0800	1116-53	1700	1116-17	1802	1124-03
T1XS3BP	0302	*1122-21	0302	1212-06	0901	1218-04
	0902	1215-46	0902	1216-72	0902	1218-18
	1802	1124-1 3				
TXS3BQ	0302	1121-24	0302	*1122-19	0400	1128-18
	0800	1116-59	0901	1215-24	1700	1116-23
	1802	1124-07				
TXS4BP	0302	*1122-35	0302	1212-07	0901	1115-22
	0901	1215-01	0901	1215-55	0902	1215-48
	0902	1216-73	0902	1218-19	1802	1124-18
TXS4BQ	0302	1121-17	0302	*1122-37	0400	1128-40
	0800	1116-77	0901	1215-06	0901	1215-61

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
	0901	1217-01	0901	121 8-05	1802	1124-24
TXS5BP	0302	*1122-33	0302	1212-08	0901	1213-33
	0901	1215-04	0901	1215-60	0901	1215-66
	0901	1218-06	0902	1216-74	1802	1124-20
TXS5BQ	0302	1121-23	0302	*1122-31	0400	1128-34
	0800	1116-71	0901	1213-41	0901	1215-08
	0901	1217-04	0902	1218-20	1802	1124-26
TXS6BP	0302	*1122-47	0302	1212-10	0901	1213-35
	0901	1213-46	0901	1215-05	0901	1215-10
	0901	1218-07	0902	1218-22	1802	1124-23
TXS6BQ	0302	1121-40	0302	*1122-49	0400	1128-54
	0800	1116-65	0901	1215-62	0901	1215-68
	0901	1217-05	0902	1216-75	1802	1124-17
TXS7BP	0302	*1122-45	0302	1212-13	0901	1215-07
	0901	1215-13	0901	1215-70	0901	1218-08
	0902	1216-77	0902	1218-24	1802	1124-25
TXS7BQ	0302	1121-30	0302	*1122-43	0400	1128-48
	0800	1116-76	0901	1213-37	0901	1213-48
	0901	1215-64	0901	1217-07	1802	1124-19
TXSCMP	0301	*1122-57	0301	1211-06	0301	1213-06
TXSCMQ	0301	*1122-55	0800	1216-04		
TXSENP	0301	*1122-76	0301	1211-08	0301	1213-08
TXSENQ	0301	*1122-78	0800	1218-46		
TXSK00	0302	1122-01	0302	1122-10	0302	1122-14
	0302	1122-26	0302	*1222-06		
TXSK10	0302	*1122-01	0302	1122-30	0302	1122-42

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
	0302	1122-46	0302	1122-56		
TXSPBP	0301	*1122-59	0301	1211-10	1802	1126-18
TXSPBQ	0301	*1122-61	0400	1128-68	0901	1216-22
	1802	1124-70				
TXSRSA	0301	1122-64	0301	1122-66	0301	1122-75
	0302	*1116-45	0302	1122-04	0302	1122-06
TXSRTA	0302	1116-51	0302	1122-20	0302	1122-22
	0302	1122-36	0302	1122-38	0302	1122-50
	0302	1122-52				
TXST0Q	0902	1117-43	0902	1119-48		
TXST1A	0700	1224-06	0902	1116-39	0902	1117-46
TXST1Q	0902	1116-35	0902	1119-43		
TXX04A	0700	1217-11	0800	1215-31	0800	1215-38
TXXA0P	0700	1118-69	0800	1216-08	0800	1216-36
	0800	1218-50	0901	1215-54	0901	1216-19
	0901	121 8-34	1802	1216-62		
TXXA0Q	0700	1118-74	0700	1119-71	0700	1217-10
TXXA1P	0302	1116-41	0302	1116-47	0700	1119-69
TXXA1Q	0700	1118-77	0700	1119-74	0800	1216-07
	0800	1216-37	0800	1218-52	0901	1215-56
	0901	1216-20	0901	1218-36	1802	1216-64
TXXA2Q	0302	1116-43	0302	1116-49	0700	1118-78
	0700	1119-77				
TXXA3P	0700	1117-72	0700	1117-79	0700	1118-60
	0700	1118-71	0700	1119-76		
TXXA3Q	0700	1119-78	0700	1217-13		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TXXACA	0301	1211-13	0301	1214-06		
TXXAC0	0301	1214-08	0302	1212-11		
TXXACP	0700	1117-69	0700	1118-73	0700	1118-75
	0700	1119-73	0700	1119-75		
TXXADA	0301	1116-52	0700	1117-73		
TXXAD0	0301	1116-54	0301	*1211-11		
TXXB0P	0700	*1117-76	0700	1217-06	0800	1216-13
	0800	1 21 8-48				
TXXB0Q	0700	*1117-78	0700	1118-62	0800	1216-34
	0901	1209-20	0901	1209-26	0901	1216-18
TXXB1P	0700	1117-77	0700	*1118-57	0700	1217-08
	0800	1215-34	0800	1215-40	0800	1216-06
	0800	1218-49	0901	1209-07	0901	1214-70
TXXB1Q	0700	*1118-55	0901	1215-52	0901	1218-31
TXXBCA	0301	*1116-46	0700	1117-75	0700	1118-64
TXXBC0	0301	1116-48	0301	*1213-04		
TXXC0Q	0600	*1202-13	0600	1203-08		
TXXC1Q	0600	*1203-13	0600	1204-08		
TXXC2P	0302	1222-04	0302	1228-08	0600	*1204-11
TXXC2Q	0600	*1204-13	0600	1205-08	0600	1213-01
TXXC3Q	0600	*1205-13	0600	1206-08		
TXXC4P	0500	1207-01	0500	1207-14	0500	1207-26
	0600	1202-08	0600	*1206-11	0600	1207-10
TXXC4Q	0600	*1206-13	0600	1213-03		
TXXCIA	0600	1207-15	0600	*1208-75		
TXXCI0	0600	1208-77	0600	*1209-75		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TXXCIP	0600	*1207-11	0600	1217-22	1802	1126-48
TXXCR0	0600	1202-06	0600	1203-06	0600	1204-06
	0600	1205-06	0600	1206-06	0600	*1217-23
TXXCSA	0600	1116-34	0600	*1213-07		
TXXCS0	0302	1121-01	0302	1121-06	0302	1121-09
	0302	1121-14	0302	1121-21	0302	1121-22
	0302	1121-29	0302	1121-38	0302	1121-52
	0600	*1116-30	0600	1121-33		
TXXDDA	0500	1207-03	0500	*1208-09		
TXXDDP	0500	*1207-09	0500	1211-04	0500	1225-24
	0600	1217-24				
TXXDDQ	0500	*1207-07	0500	1209-54		
TXXDDR	0500	1224-22	0500	*1225-20	1001	1218-77
TXXDDS	0500	1208-03	0500	*1224-20	0500	1225-22
TXXDIA	0500	1207-27	0500	*1208-15	1400	1230-36
TXXDIP	0500	*1207-23	0500	1209-56	0500	1211-05
	0500	1225-18	0600	1217-25	0800	1208-17
TXXDIQ	0500	1123-55	0500	1123-61	0500	1123-64
	0500	1123-70	0500	1123-73	0500	1123-74
	0500	1123-78	0500	1123-79	0500	*1207-25
TXXDIR	0500	1224-14	0500	*1225-19	1001	1218-74
TXXDIS	0500	1208-13	0500	*1224-19	0500	1225-14
TXXDSP	0500	*1207-2'1	0500	1211-07	0600	1217-26
TXXDSQ	0500	1123-31	0500	1123-36	0500	1123-37
	0500	1123-42	0500	1123-43	0500	11 23-49
	0500	1123-50	0500	1123-56	0500	*1207-19

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
TXXR0Q	0600	*1117-61	0600	1118-68	0600	1213-45
TXXR1Q	0600	*1118-61	0600	1119-68		
TXXR2P	0600	1117-68	0600	*1119-59	0600	1122-72
TXXRCA	0600	1122-60	0600	*1214-60		
TXXRC0	0600	1214-62	0600	*1218-59		
TXXRCQ	0600	1117-66	0600	1118-66	0600	1119-66
	0600	*1122-74				
TXXREP	0600	*1128-57	0600	1214-64		
XBEH0A	2101	XA4-17	2400	*XA5-16		
XB0T1A	2102	A10A1-F2	2102	A1J2-63	2102	W3P2-63
	2102	*XA4-11	2700	W3P1-37	2700	W3P2-63
XB0T1A1	1900	1133-61	1900	1135-23	1900	*1136-37
	1900	1231-75				
XB0T1AR	1900	1133-58	1900	1136-38	2102	*A100A1-F3
	2102	A1 J2-64	2102	W2P2-64	2700	W3P1-38
	2700	W3P2-64				
XB0TIN	2400	A10A1-V7	2400	A7CR2-C	2400	*XA5-38
XB0TSS	2101	XA4-38	2102	XA4-38	2400	*XA5-17
	2400	XA5-40				
XCRSTAV	2102	*XA4-26	2400	XA5-02		
XDRIVA	2400	A10A1-W5	2400	A10P2-D	2400	*XA5-22
XDRIVB	2400	A10A1-W4	2400	A10P2-F	2400	*XA5-20
XENH0A	2101	XA4-35	2400	*XA5-11		
XE0T1A	2102	A10A1-F5	2102	A1J2-65	2102	W3P2-65
	2102	*XA4-12	2700	W3P1-39	2700	W3P2-65
XE0T1A1	1900	1133-62	1900	1135-25	1900	*1136-39

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
	1900	1231-71				
XE0T1AR	1900	1133-58	1900	1136-40	2102	*A10A1-F4
	2102	AlJ2-66	2102	W2P2-66	2700	W3P1-40
	2700	W3P2-66				
XE0TFS	2101	XA4-34	2102	XA4-34	2400	*XA5-03
	2400	XA5-39				
XE0TIN	2400	A10A1-V8	2400	A7CR1-C	2400	*XA5-41
XETML0	2400	Al A2Q4-C	2400	A1 A9J 1 -M	2400	Al A9P3-d
	2400	*A1J3-d				
XFPRSA	1201	AlJ2-67	2102	A10A1-H4	2102	A1J2-67
	2102	W3P2-67	2102	*XA4-05	2700	W3P1-41
	2700	W3P2-67				
XFPRSA1	1201	1133-59	1201	1135-38	1201	*1136-41
XFPRSAR	1201	1133-58	1201	1136-42	2102	*A1 0A1-H3
	2102	A1 J2-68	2102	W3P2-68	2700	W3P1-42
	2700	W3P2-68				
XFSTFQ	2101	*XA4-19	2400	XA5-33		
XFSTR0	2101	*XA4-41	2400	XA5-37		
XFWDC0	2101	*XA4-20	2400	XA5-35		
XH0LSS	2400	*A1 0A1 -V1	2400	A8A1-E	2400	XA5-19
XHSLED	2400	*A1 0A1-W2	2400	A8A3-C	2400	A8A5-C
	2400	XA5-01				
XLDFFS	2101	XA4-30	2400	*XA5-10		
XL0TSS	2400	*A10A1-V6	2400	A8A2-E	2400	XA5-32
XLSWNC	2400	*A10A1-X4	2400	A7S2-NC	2400	XA5-06
XLSWN0	2400	*A10A1-X3	2400	A7S2-N0	2400	XA5-09

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
XMTRDA	2400	AlA1Q2-C	2400	AlA1Q5-C	2400	*AlA2-01
	2400	A1A2CR3-A	2400	A1A9J2-A		
XMTRDB	2400	A1AlQ3-C	2400	A1A1Q6-C	2400	*A1A2-03
	2400	A1A2CR4-A	2400	AlA9J2-C		
XRCHLC	2300	A10A1-U1	2300	*J1-R		
XRCHLH	2300	*J1-V	2300	XA3-37		
XRCHIL	2300	*J1-S	2300	XA3-36		
XRCH2C	2300	A10A1-U1	2300	*J1-B		
XRCH2H	2300	*J1-F	2300	XA3-39		
XRCH2L	2300	*J1-C	2300	XA3-38		
XRCH3C	2300	A10A1-U1	2300	*J1-d		
XRCH3H	2300	*J1l-f	2300	XA3-40		
XRCH3L	2300	*J1-c	2300	XA3-41		
XRCH4C	2300	A10A1-U1	2300	*J1-E		
XRCH4H	2300	*J1-A	2300	XA2-37		
XRCH4L	2300	*J1-D	2300	XA2-36		
XRCH5C	2300	A10A1-U1	2300	*J1-X		
XRCH5H	2300	*J1-Z	2300	XA2-39		
XRCH5L	2300	*J1-W	2300	XA2-38		
XRCH6C	2300	A10A1-U1	2300	*J1-U		
XRCH6H	2300	*J1-P	2300	XA2-40		
XRCH6L	2300	*J1-T	2300	XA2-41		
XRCH7C	2300	A10A1-U1	2300	*J1-M		
XRCH7H	2300	*J1-L	2300	XA1-37		
XRCH7L	2300	*J1-H	2300	XA1-36		
XRCH8C	2300	A10A1-U1	2300	*J1-J		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
XRCH8H	2300	*J1-K	2300	XA1-39		
XRCH8L	2300	*J1-N	2300	XA1-38		
XRCH9C	2300	A10Al-U1	2300	*J1-a		
XRCH9H	2300	*J1-b	2300	XA1-40		
XRCH9L	2300	*J1-Y	2300	XA1-41		
XRDB0A	2300	A10A1-A1	2300	A1J2-03	2300	*XA1-21
	2700	W3P1-03	2700	W3P2-03		
XRDB0A1	1300	1133-11	1300	1135-08	1300	*1136-03
XRDB0AR	1300	1133-16	1300	1136-04	2300	*A10A1-B3
	2300	A1J2-04	2700	W3P1-04	2700	W3P2-04
XRDB1A	2300	A10Al-B1	2300	A1J2-05	2300	*XA2-16
	2700	W3P1-05	2700	W3P2-05		
XRDB1A1	1300	1133-06	1300	1135-10	1300	*1136-05
XRDB1AR	1300	1133-02	1300	1136-06	2300	*A10A1-B2
	2300	A1 J2-06	2700	W3P1-06	2700	W3P2-06
XRDB2A	2300	A10A1-C7	2300	A1J2-07	2300	*XA2-18
	2700	A1 J2-07	2700	W3P1-07	2700	W3P2-07
XRDB2A1	1300	1133-04	1300	1135-05	1300	*1136-07
XRDB2AR	1300	1133-02	1300	1136-08	2300	*A10A1-B6
	2300	A1J2-08	2700	W3P1-08	2700	W3P2-08
XRDB3A	2300	A10A1-C4	2300	A1J2-09	2300	*XA3-16
	2700	W3P1-09	2700	W3P2-09		
XRDB3A1	1300	1133-05	1300	1135-07	1300	*1136-09
XRDB3AR	1300	1133-02	1300	1136-10	2300	*A10A1-C3
	2300	A1J2-10	2700	W3P1-10	2700	W3P2-10
XRDB4A	2300	A10A1-A3	2300	A1J2-11	2300	*XA1-16

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
	2700	W3P1-17	2700	W3P2-11		
XRDB4A1	1300	1133-09	1300	1135-09	1300	*1136-17
XRDB4AR	1300	1133-16	1300	1136-18	2300	*A10A1-B5
	2300	A1J2-12	2700	W3P1-18	2700	W3P2-12
XRDB5A	2300	A10Al-D1	2300	A1J2-13	2300	*XA3-21
	2700	W3P1-19	2700	W3P2-13		
XRDB5A1	1300	1133-15	1300	1135-20	1300	*1136-19
XRDB5AR	1300	1133-32	1300	1136-20	2300	*A10A1-D2
	2300	A1J2-14	2700	W3P1-20	2700	W3P2-14
XRDB6A	2300	A10A1-A2	2300	AlJ2-15	2300	*XA1-18
	2700	W3P1-21	2700	W3P2-15		
XRDB6A1	1300	1133-22	1300	1135-26	1300	*1136-21
XRDB6AR	1300	1133-16	1300	1136-22	2300	*A10A1-B4
	2300	A1J2-16	2700	W3P1-22	2700	W3P2-16
XRDB7A	2300	A10A1-C5	2300	A1J2-17	2300	*XA3-18
	2700	W3P1-23	2700	W3P2-17		
XRDB7A1	1300	1133-23	1300	1135-24	1300	*1136-23
XRDB7AR	1300	1133-32	1300	1136-24	2300	*A10A1-C6
	2300	A1J2-18	2700	W3P1-24	2700	W3P2-18
XRDBPA	2300	A10A1-C1	2300	A1J2-1	2300	*XA2-21
	2700	W3P1-25	2700	W3P2-01		
XRDBPA1	1300	1133-20	1300	1135-17	1300	*1136-25
XRDBPAR	1300	1133-32	1300	1136-26	2300	*A10A1-C2
	2300	A1 J2-02	2700	W3P1-26	2700	W3P2-02
XRDBSA	2300	A10A1-D4	2300	A1J2-19	2300	*XA3-20
	2700	W3P1-33	2700	W3P2-19		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
XRDBSA1	1300	1133-47	1300	1133-52	1300	1135-19
	1300	*1136-33				
XRDBSAR	1300	1133-44	1300	1136-34	2300	*A10A1-D3
	2300	A1J2-20	2700	W3P1-34	2700	W3P2-20
XRDCLAV	2102	*XA4-32	2300	XA1-24	2300	XA2-24
	2300	XA3-24				
XRDC0M	2300	*A10A1-U1	2300	XA1-35	2300	XA2-35
	2300	XA3-3:5				
XRDY1A	1001	1135-36	1001	1136-35	2102	A10A1-F7
	2102	A1 J2-61	2102	W3P2-61	2102	*XA4-04
	2700	W3P1-35	2700	W3P2-61		
XRDY1A1	1001	1133-55	1001	1135-36	1001	*1136-35
XRDY1AR	1001	1133-67	1001	1136-36	2102	*A100A1-F6
	2102	A1J2-62	2102	W3P2-62	2700	W3P1-36
	2700	W3P2-62				
XREVRQ	2101	*XA4-08	2400	XA5-34		
XREW1A	2102	1135-40	2102	1136-31	2102	A1 0A1-H1
	2102	AIJ2-69	2102	W3P1-31	2102	W3P2-69
	2102	*XA4-10	2700	W3P1-31	2700	W3P2-69
XRN0DE	2102	XA4-36	2300	*XA1-22	2300	*XA2-22
	2300	*XA3-22				
XRRSTAV	2102	*XA4-03	2300	XA1-23	2300	XA2-23
	2300	XA3-23				
XRSTB0V	2102	*XA4-40	2300	XA3-17		
XSENSA	2400	A10A1-V4	2400	*A10P2-H	2400	XA5-31
XSENSB	2400	A10A1-V2	2400	*A10P2-K	2400	XA5-28

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
XSGATA	2102	*XA4-23	2300	XA1-19	2300	XA2-19
	2300	XA3-19				
XSTPSS	2400	*A10A1-W6	2400	A8A4-E	2400	XA5-23
XTACHD	2400	A10A1-V3	2400	A10P2-B	2400	A1A2-05
	2400	A1A9J1-B	2400	*A1A9J2-D	2400	A1A9P3-L
	2400	A1J3-L	2400	XA5-21		
XTACHR	2400	A10A1-V5	2400	A10P2-E	2400	AlA2-04
	2400	A1A9J1-E	2400	*A1A9J2-B	2400	A1A9P3-H
	2400	A1J3-H	2400	XA5-25		
XWCH1H	2200	A10J2-e	2200	*XA3-01		
XWCH1L	2200	A100J2-c	2200	*XA3-04		
XWCH2H	2200	A10J2-V	2200	*XA3-02		
XWCH2L	2200	A10J2-S	2200	*XA3-05		
XWCH3H	2200	A10J2-T	2200	*XA3-06		
XWCH3L	2200	A10J2-P	2200	*XA3-03		
XWCH4H	2200	A10J2-N	2200	*XA2-01		
XWCH4L	2200	A100J2-K	2200	*XA2-04		
XWCH5H	2200	A10J2-H	2200	*XA2-02		
XWCH5L	2200	A10J2-L	2200	*XA2-05		
XWCH6H	2200	A10J2-A	2200	*XA2-06		
XWCH6L	2200	A10J2-D	2200	*XA2-03		
XWCH7H	2200	A10J2-F	2200	*XA1-01		
XWCH7L	2200	A10J2-C	2200	*XA1-04		
XWCH8H	2200	A10J2-V	2200	*XA1-02		
XWCH8L	2200	A10J2-b	2200	*XA1-05		
XWCH9H	2200	A10J2-Z	2200	*XA1-06		

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
XWCH9L	2200	A10J2-W	2200	*XA1-03		
XWRCLK	2200	*XA1-28	2200	XA2-28	2200	XA3-28
XWRERC	2102	*XA4-18	2200	A100J2-B	2200	A10J2-E
	2200	A10J2-J	2200	A10J2-M	2200	A10J2-R
	2200	A10J2-U	2200	A100J2-X	2200	A10J2-a
	2200	A10J2-d	2200	A100J2-f		
XWRITE	2102	*XA4-01	2200	XA1-07	2200	XA2-07
	2200	XA3-07				
XWRSTA	2102	*XA4-02	2200	XA1-09	2200	XA2-09
	2200	XA3-09				
ZRQ0GB	0301	*W2J1-W	0301	W2S9C-01	2502	*W2J1-W
	2502	W2S9C-01				
ZRQ0HB	0301	*W2J1-V0301 ' W2S9B-01			2502	*W2J1-V
	2502	W2S9B-01				
ZRQ1GB	0301	*W2J1-Y	0301	W2S9C-02	2502	*W2J1-Y
	2502	W2S9C-02				
ZRQ1HB	0301	*W2J1-X	0301	W2S9B-02	2502	*W2J1-X
	2502	W2S9B-02				
ZRQ2GB	0301	*W2J1-a	0301	W2S9C-03	2502	*W2J1-a
	2502	W2S9C-03				
ZRQ2HB	0301	*W2J1-Z	0301	W2S9B-03	2502	*W2J1-Z
	2502	W2S9B-03				
ZRQ3GB	0301	*W2J1-c	0301	W2S9C-04	2502	*W2J1-c
	2502	W2S9C-04				
ZRQ3HB	0301	*W2J1-b	0301	W2S9B-04	2502	*W2J1-b
	2502	W2S9B-04				

Table 5-2. Key Signal Lookup Listing - Continued

Signal	Distribution					
ZRQ4GB	0301	*W2J1-e	0301	W2S9C-05	2502	*W2J1-e
	2502	W2S9C-05				
ZRQ4HB	0301	*W2J1-d	0301	W2S9B-05	2502	*W2J1-d
	2502	W2S9B-05				
ZRQ5GB	0301	*W2J1-g	0301	W2S9C-06	2502	*W2J1-g
	2502	W2S9C-06				
ZRQ5HB	0301	*W2J1-f	0301	W2S9B-06	2502	*W2J1-f
	2502	W2S9B-06				
ZRQ6GB	0301	*W2J1-i	0301	W2S9C-07	2502	*W2J1-i
	2502	W2S9C-07				
ZRQ6HB	0301	*W2J1-h	0301	W2S9B-07	2502	*W2J1-h
	2502	W2S9B-07				
ZRQ7GB	0301	*W2J1-k	0301	W2S9C-08	2502	*W2J1-k
	2502	W2S9C-08				
ZRQ7HB	0301	*W2J1-j	0301	W2S9B-08	2502	*W2J1-j
	2502	W2S9B-08				

Section II. OVERALL THEORY OF OPERATION

5-6. Overall Functional Description (fig. 5-4). The magnetic type unit (MTU) is a peripheral device for storage and subsequent retrieval of computer program data supplied by the automatic data processor (ADP). The MTU normally operates automatically on instructions from the ADP to record or reproduce digital data from magnetic tape contained in a removable tape cartridge. The data and control information is transmitted through an input/output exchange (IOX 1) channel capable of servicing up to seven additional peripheral devices. The MTU is assigned a device address that permits the ADP to select only the MTU from the possible eight devices connected to this channel. Once selected, the MTU is completely controlled by the ADP to provide its basic read or write functions, or any special functions such as erase and high speed forward. In addition to normal automatic (on-line) operation, the MTU also can be operated manually (off-line) to provide test read, and wind/rewind functions.

a. ADPIMTU Interface. Communications between the ADP and MTU are provided over nine parallel information lines, carrying data bits 0 through 7 and parity. The information lines carry the data to be recorded or retrieved from tape and MTU control functions such as address selection, device control, and device commands. The first eight information lines (O through 7) contain the data in the form of 8-bit bytes. The ninth line provides an odd-parity bit used during actual data transmission. In controlling communications between the ADP and MTU, four additional lines are also used; a request line, enable line, command line, and indicator line. The MTU activates the request line to inform the ADP, through the assigned MTU channel, that the device is requesting service. The ADP responds to this request, at the appropriate time, by addressing the MTU while activating the enable line. The MTU can then send and receive data. The command function, however, is initiated by the ADP when it requires the MTU to perform a specific operation such as read or write. The ADP performs this function by addressing the MTU while activating the command line. After receiving the actual command, the MTU activates the indicator line to acknowledge its receipt.

b. MTU Operating Modes. The MTU operates in two basic modes; on-line and off-line. On-line operation is automatic, with complete control provided by the ADP. Off-line operation inhibits the ADP input and permits manual operation.

(1) *On-line mode*. This mode is selected with ON-LINE switch S2. Actuation of switch S2 lights the ON-LINE indicator and inhibits the self-test, manual tape forward, and manual tape rewind logic functions. If the tape cartridge is installed in magnetic tape transport (MTT) Al, and the MTT access door is closed, a ready status signal is applied from the MTT to logic section A2. This signal, combined with the on-line signal, produces a ready status signal which lights READY indicator DS 1. After generation of the ready status signal, the ADP controls all functions with the exception of the erase/write function. The erase/write function comes under ADP automatic control when WRITE ENABLE switch S3 is actuated and the writeprotect cam switch on the tape cartridge is inhibited. With the cam switch inhibited, a write enable status signal is applied to logic section A2, and is combined with the front panel write enable and online switch inputs. This results in generation of a write enable status signal, which activates the internal MTU write circuits and lights the WRITE ENABLE indicator. Data can then be recorded on the tape under command of the ADP.

(2) *Off-line mode*. Resetting the ON-LINE switch removes the ADP control and permits the MTU to be operated manually (off-line) for test purposes and tape cartridge removal and replacement. With the ON-LINE switch reset, the ONLINE indicator is off and the write logic in the A2 assembly is inhibited, which turns off the READY and WRITE ENABLE indicators. The off-line mode also inhibits all data and control inputs from the ADP, while removing the inhibit levels from the self-test, tape forward, and tape reverse switch logic. Removing these inhibits enables the TEST, FORWARD, and REWIND switch functions.

(a) *FORWARD switch*. Actuation of the FORWARD switch (S6) enables the forward motion logic in the A2 assembly, which sends high speed, forward, and run commands to the MTT. The combination of the run and forward signals also enables the forward status output to light the FORWARD indicator. The MTT responds by winding the tape forward at high speed until the end of tape (EOT) marker is sensed. The MTT then trans-

mits an EOT status signal to the A2 assembly. This signal resets the run logic and lights the EOT indicator. With the run logic reset, a stop command is applied to the MTT, causing forward tape motion to stop. The reset condition also inhibits the forward status output from the A2 assembly, which turns off the FORWARD indicator.

(b) *REWIND switch*. Actuation of the REWIND switch (S7) lights the REWIND indicator; enables the reverse-motion logic; and sends highspeed, reverse, and run commands to the MTT. The MTT rewinds the tape at high speed until the beginning of tape (BOT) marker is sensed. The MTT transmits a BOT status signal that resets the run logic and lights BOT indicator DS2. The reset logic also applies a stop command to the MTT, stopping reverse motion and turning off the REWIND indicator. In addition to the manual tape forward/ rewind functions, a manual test function is also provided to permit a parity check to be made on the next record of data read from tape.

(c) *TEST switch*. Actuation of TEST switch (S8) enables the test-condition logic in the A2 assembly, which responds by applying read permit, run, low speed, and forward commands to the MTT. If the MTT is in a ready condition, the next record of data is read in the forward direction, and each byte is strobed onto the read data lines. A read-strobe pulse then loads each byte of data into the read register of the A2 assembly. The. parity check logic then checks each byte for parity error. A parity error causes the FAULT indicator to light. After the last data byte is read, an interrecord gap (IRG) is sensed by the gap detect logic, and a stop command is applied to the MTT. The stop command stops the tape motion with the magnetic head positioned in the interrecord gap.

c. Data Format. The ADP supplies data in the form of 9-bit bytes that are magnetically recorded in channels across the tape by a nine-channel record head. The recorded data is organized into logical groups called records, with a record consisting of up to 32,768 bytes. Records are further subdivided into blocks composed of a varying number of bytes, up to a maximum of 2048. Records can, therefore, consist of from one to a maximum of 16 blocks (32,768/2048=16).

(1) *Write operation*. In an operation such as write, an end of block (EOB) counter in the A2 assembly is initially preset to the number of blocks required. The ADP then issues an EOB command decrements the EOB counter by one until the EOB counter is at zero. The next EOB command received then initiates a write terminate operation. This consists of writing a longitudinal redundancy check (LRC) byte, generating an interrecord gap (31/4 to 3-1/2 in. maximum of blank tape), and initiating an interrupt sequence.

(2) *Interrupt sequence*. The interrupt sequence is initiated at the MTU by generating a request to the ADP. At an appropriate time in ADP operations, the MTU is addressed and the enable line is activated. The MTU responds by activating the indicator line and sending an interrupt status to acknowledge receipt of the enable function. If another write command is not received within 5 ms, a stop sequence is initiated, and the MTU reverts to the standby state.

Section III. DETAILED DESCRIPTION

5-7. General (fig. 5-5). During normal, on-line operation, the magnetic tape unit (MTU) records and reproduces automatic data processor (ADP) digital data on commands from the ADP. The MTU is therefore an external memory for the ADP. For on-line operation to occur, the *on-line* signal from the front panel is sent to the test command generator which in turn distributes an *on-line* enabling signal throughout the MTU. *The I/IO bus* between the ADP and the MTU carries command, read, and write data. The *request* signal line carries the response of the MTU to the ADP. The number of the *request* signal line (O thru 7) is determined by the request channel selected on the front panel. The *indicator* signal line from the MTU to the ADP indicates receipt of a special command or an interrupt. The *command (CMD)* or *enable* signals, accompanied by an address bit over the *I/0 bus*, address the MTU. The *CMD* signal line is also used simultaneously with the *enable* signal line from the ADP to produce the *master reset* signal. The *enable* signal is the response of the ADP to the MTU request and causes one byte to be transferred. The *master reset* signal causes the MTU to go into a

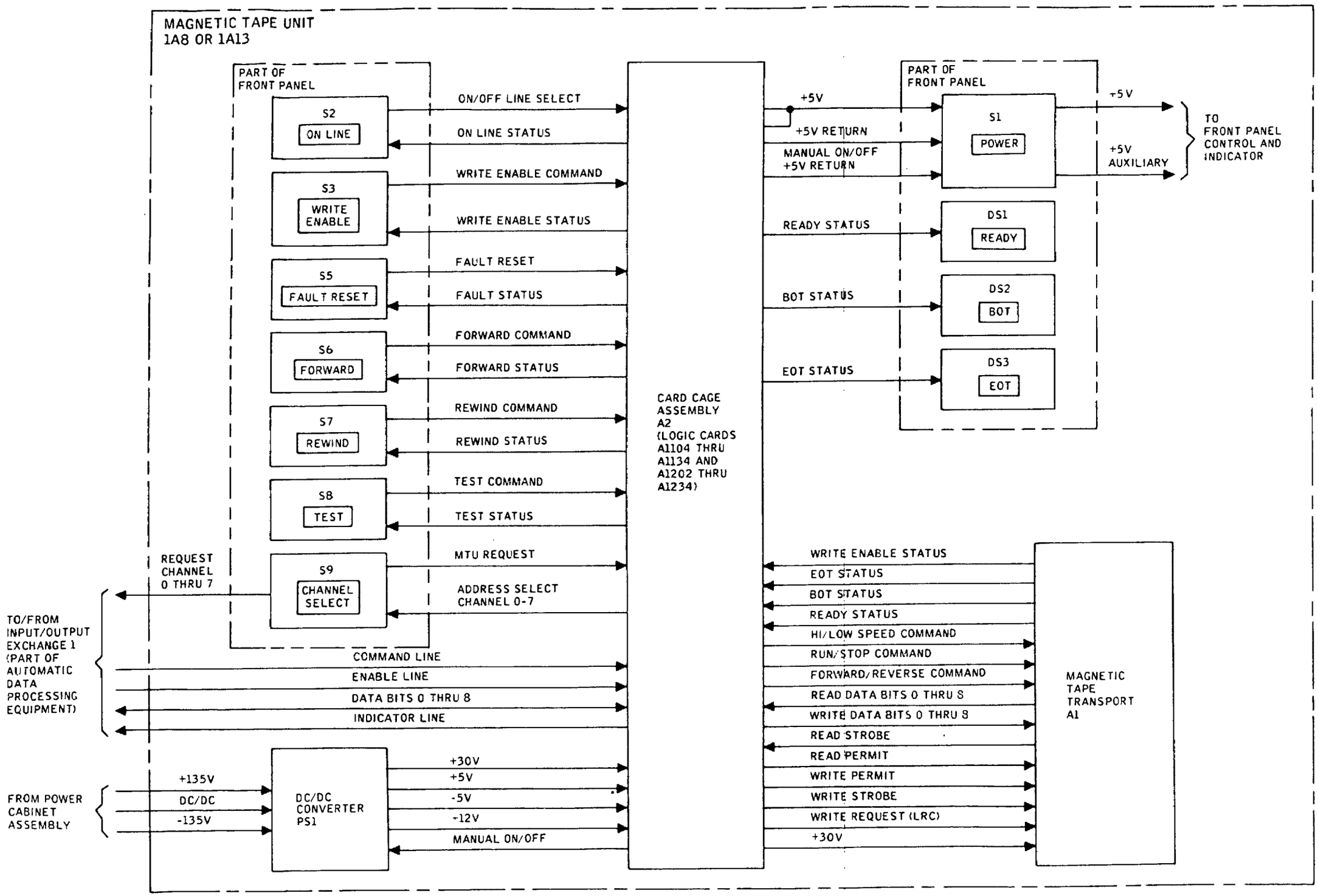


Figure 5-4. MTU Overall Block Diagram

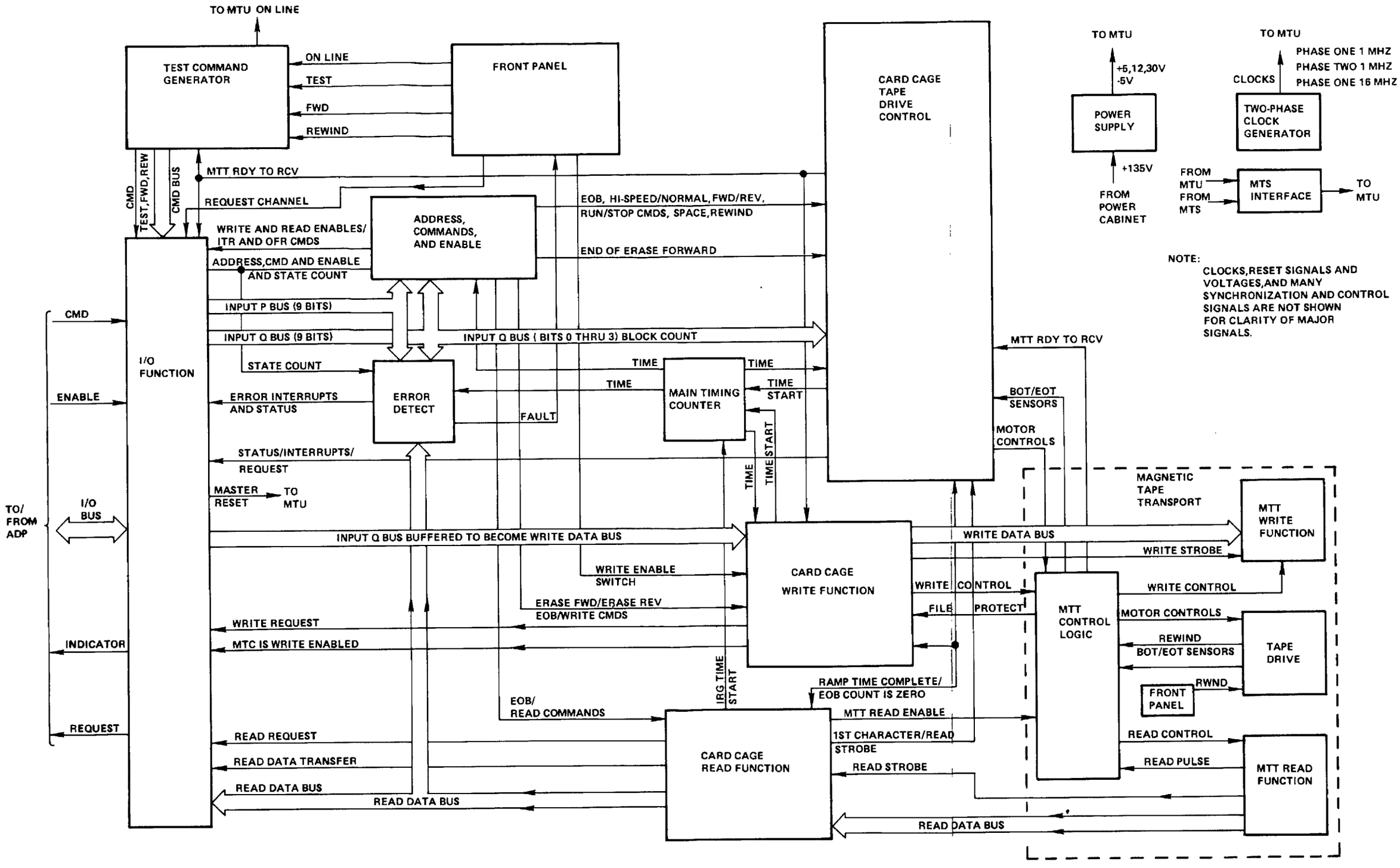


Figure 5-5. MTU Functional Block Diagram

standby state. When the test mode is selected on the front panel, the test signal is sent to the test command generator. The test command generator then sends an MTU signal on the CMD bus and another CMD signal on its dedicated line to the I/O function. However, the on-line mode must be disabled on the front panel for the test command to be generated. Selection of the forward or rewind functions on the front panel causes the test command generator to provide a forward (FWD) or rewind (REW) command signal to the I/O function. If the rewind function is selected, the magnetic tape transport (MTT) rewinds the tape to the beginning. The rewind (RWND) signal goes to the tape drive in the MTT. The tape drive sends the rewind signal to the MTT control logic. The rewind signal causes the MTT control logic to send the motor controls signal to the tape drive for positioning the tape at the beginning of the reel. The state count signal from the I/O function indicates to the error detect and the address, commands, and enable circuits whether the input Q bus is sending command or write data. The command operations data generated in response to the ADP are as follows:

Output-from-register command (OFR CMD)
Input-to-register command (ITR CMD)
End-of-block command (EOB CMD)
Stop command (stop CMD)
Device command (DEV CMD)

a. OFR CMD. The OFR CMD is used by the ADP to generate a known data pattern for the MTU. The OFR CMD consists of an active command line and an address selection byte followed by a control byte. The bytes are received by the I/O function and sent to the address, commands, and enable function which decodes the control byte and sends the OFR CMD to the I/O function. The OFR CMD initiates a loop test within the I/O function. The OFR CMD is followed by a transfer of four data bytes from the ADP to the MTU. The MTU uses only the first data byte and disregards the other three. The MTU responds to the loop test by sending a request to the ADP. The ADP responds with an enable that causes the MTU to transfer the same byte back to the ADP. By manipulating the bit pattern, all data lines can be checked.

b. ITR CMD. The error detect block and the card cage tape drive control block provide operational status and error status signals, respectively, to a register in the I/O function. The ITR CMD is used by the ADP to read out the status contents of the register. The ITR CMD consists of the address byte followed in sequence by the control byte and the transfer of the status byte from the register to, the ADP. The indicator line is activated when the last data byte is sent. An error condition will initiate an interrupt sequence except when executing high speed forward or reverse. A new command resets the error status register. Error interrupts are as follows:

(1) *Tape parity error.* This error indicates the detection of a lateral or longitudinal parity error on tape during the previous read operation. When detected, the byte in error is transmitted with correct parity and the read operation continues to the end of the record. At that point an interrupt is: transmitted.

(2) *No data.* This error either indicates no data has been detected on the tape during a tape forward operation for the time equal to about 24,000 bytes as determined by the main timing counter, or it indicates that no data has been detected by the read-after-write circuit in the read function during a write operation.

(3) *Beginning of tape (BOT).* The BOT sensor signal originates in the tape drive and goes through the MTT control logic to the card cage tape drive control. The tape drive control initiates an interrupt to the I/O function.

(4) *End of tape (EOT).* The EOT error interrupt functions the same as the BOT.

(5) *Computer data parity error.* A parity error is detected in the input command data from the ADP during a write command.

(6) *File protect error.* This error indicates a write or erase command was received when the MTU was not write enabled.

(7) *Timing error.* This error indicates the ADP did not respond with data in time for a write mode or did not accept data in time for a read mode. The interrupt sequence starts with a request from the I/O function to the ADP. The ADP responds with an address enable that causes the transfer of the error status and the indicator signal from the I/O function to the ADP.

c. EOB CMD. The EOB CMD is used to decrement the EOB counter in the card cage tape drive control. The EOB CMD consists of an address byte followed by the control byte which is sent to the address, command, and enable function from the /O function. The control byte is decoded and the EOB CMD is sent to the EOB counter in the card cage tape drive control block. The EOB CMD also 'goes to the card cage read and write functions in the form of EOB/read commands and EOB/write commands.

d. Stop CMD. The stop sequence consists of an address byte followed by a control byte to the address, command, and enable function from the I/O function. The control byte is decoded and sent to the card cage tape drive control block which sends the time start signal to the main timing counter. The counter sends back the time signal after a delay that allows the tape motion to stop slowly. At the same time the stop motor control signal goes to the MTT control logic which forwards the stop motor control signal to the tape drive. The stop sequence can be initiated by the ADP as a result of the ITR CMD interrupt sequence described in paragraph 5-7b. When the stop sequence occurs as a result of an interrupt during Write or read operation, the I/O function generates S master reset which places the MTU in a standby state.

e. Device Command. There are nine device commands. Any device command consists of an address byte accompanied by the active command line, a control byte that determines if it is a device command, and a third byte that determines which one of the nine device commands is commanded. The third byte also provides the present count for the EOB counter. For example, when the ADP loads : a program, bits 4 thru 7 of the third byte command the read function, and bits 0 thru 3 preset the EOB counter. The indicator signal is generated by the I/O function after the third command byte. The nine device commands are as follows:

(1) *Write CMD*
(2) *Read CMD*
(3) *Space forward CMD*
(4) *Space reverse CMD*
(5) *Erase forward CMD*
(6) *Erase reverse CMD*
(7) *High speed forward CMD*
(8) *High speed reverse CMD*
(9) *Rewind to load point CMD.*

The three command bytes are received over the I/O bus from the ADP to the I/O function. The three bytes are then transferred to the address, command, and enable function over the input Q bus and the input P bus. The P bus is equivalent to an inverted Q bus. The block count for the EOB counter contained in the third byte continues along the input Q bus (0 thru 3) to the card cage tape drive control. The two input busses also go to the error detect block which produces an interrupt if an error exists. The address, commands, and enable function decodes the command bytes and sends the write CMD or erase CMD to the card cage write function. It also sends the run CMD, FWD CMD, normal CMD, or high speed CMD to the card cage tape drive control. The read command goes to the MTT read function and the run CMD, FWD CMD, normal CMD, or high speed CMD goes to the card cage tape drive control. The other device commands go to the card cage tape drive control which generates the motor controls for all commands. The motor controls go to the MTT control logic which in turn sends them to the tape drive. The motor controls go to the MTT control logic which produces motor controls for the tape drive. The tape cartridge must be in place, with the MTT door closed, for a ready condition. When ready, the MTT control logic sends the MTT ready-to-receive (RDY to-RCV) signal through the card cage tape drive control to the test command generator, card cage write function, and I/O function. In addition, during write operation, the write enable switch signal from the MTU front panel to the card cage write function must be activated, and the file protect signal from the MTT control logic must be disabled. The card cage write function then sends the MTC is write enabled signal to the I/O function.

(1) *Write and read commands*. The card cage tape drive control receives the run CMD, FWD CMD, normal CMD, or high speed CMD and sends a time start signal to start the main timing counter. Simultaneously, the motor controls signals go through the MTT control logic to the tape drive. When the main timing counter has run long enough to allow the tape drive to ramp up to operating speed, it sends a time signal back to the tape drive control which produces the ramp time complete signal for the card cage write function or the card cage read function. Bits 0 thru 3 of the third command byte go to the tape drive control where they preset the EOB counter to the number of EOB

commands to be ignored (up to 15 commands). As the read or write operation is in progress, the ADP generates EOB commands that are decoded and sent to the tape drive control and card cage write and read functions. The EOB counter in the tape drive control is decremented from the original count by each EOB CMD. When the count reaches zero, the EOB count is zero signal from the card cage to the read or write function is achieved. When the next EOB CMD is coincident, the read or write operation is terminated.

(a) *Write CMD.* When the write command has been received, the write function then generates a request to the I/O function. The I/O function then forwards the request to the ADP. The ADP responds with an addressed enable that goes through the I/O function to the address, commands, and enable function. There it is decoded and sent back to the I/O function. As a result of the enable, the write data is received from the ADP over the I/O bus to the I/O function. Within the I/O function the input Q bus is buffered to produce the write data bus to the card cage write function. The write function contains a counter that controls the rate that the write data is transferred over the write data bus to the MTT write function where the data is recorded on tape. The rate is one byte every 50 is. This is also the rate that a new byte is requested by the write request signal to the I/O function. The request address enable-one data byte sequence continues until the EOB CMD and the EOB count is zero signals are coincident. This starts the write terminate sequence which consists of a longitudinal redundancy check (LRC) delay after the last write byte. Following the LRC delay the MTT write function is reset by a write reset signal sent over the write control lines through the MTT control logic to the MTT write function. This reset results in the written LRC character. The erase head is always on when the write operation is in progress. As the tape continues to move with no write data, an interrecord gap (IRG) is created. The read function reads while writing and sends the IRG start time signal to the main timing counter for each byte it reads. It simultaneously sends the 1st character signal for each byte it reads to the IRG circuits in the tape drive control. When no 1st character signal is received (no data on tape) for the time established by the time signal from the main timing counter to the tape drive control, an interrupt is generated by the tape drive control for transfer to the I/O function. The interrupt is used within the tape drive control to start a 5-ms delay. At the completion of the delay the card cage tape drive controlled stop sequence is initiated. Also, as data is sent over the write data bus, if a byte is not present at the proper time in the card cage write function, a timing error is detected and a write terminate is initiated. If another command is received within 5 ms, the tape continues; if not, a stop sequence occurs. The data on the tape is organized into logical groups called records. The record length is determined by the block length field of the I/O key word in the ADP and the block length field of the device command word in the ADP. The maximum record length is 2,048 by 16 bytes (equivalent to 8,192 32-bit ADP words) which is equivalent to 32,768 8-bit bytes (about 41.0 inches on the MTU tape). One byte written every 50 tIs equals 20,000 bytes per sec; therefore, 32,768 bytes takes 1.64 sec. The tape runs at 25 ips; therefore, 1.64 sec times 25 ips is equal to 40.96 in.

(b) *Read CMD.* The card cage read function receives the read command through the I/O function and the address, commands, and enable function. At the same time, the card cage tape drive control sends the FWD CMD and normal CMD motor control signals to the tape drive through the MTT control logic. The main timing counter provides the time signal for the tape drive to ramp up to speed. Then the card cage read function receives the ramp time complete signal from the tape drive control. When the ramp time is complete, the card cage read function sends the MTT read enable to the MTT control logic. When the tape moves, read data is detected by the MTT read function. A read pulse is sent to the MTT control logic which in turn responds with the read control signals to the MTT read function. The MTT read function generates a read strobe that is sent to the card cage read function. The read strobe causes the transfer of read data over the read data bus. The card cage read function generates a read data transfer signal that strobes the read data over the read data bus to the I/O buffer in the I/O function. At the same time a read request is sent through the '/0 function to the ADP. The ADP responds with an addressed enable that goes to the address, commands, and enable function over the I/O bus and the address enable lines through the I/O function. The decoded read enable is sent back to the I/O function to transfer the read data from the I/O function to the ADP over the I/O bus. This sequence, that commences following the detection of each byte, is repeated for each byte. As with the write command, bits 0 thru 3 of the third read command byte specify the number of EOB commands to be disregarded. When the card cage

read function receives an EOB CMD coincident with the EOB count is zero signal, no more requests are generated; therefore, no more data is sent to the ADP. However, the tape continues to run and data is read until an IRG occurs. Each byte that is read starts the main timing counter with the IRG time start signal. At the same time, the 1st character signal goes to the card cage tape drive control. As long as data bytes are read from the tape, the timer cannot time out. When the IRG occurs, no data bytes are read and the timer sends a time signal to the card cage tape drive control that, along with the 1st character signal previously sent initiates an interrupt to the I/O function. Within the tape drive control the interrupt initiates the stop sequence. If another device command of the same speed and direction is received within 5 ms the tape continues. If not, the tape stops with the heads positioned in the IRG.

(2) *Space forward and reverse CMD.* The principles of operation for both forward and reverse commands are the same. Bits 0 thru 3 of the third command byte to the card cage tape drive control set the EOB with the number of IRG's to be ignored before stopping the tape. The decoded space CMD, FWD CMD, and normal CMD are received by the tape drive control through the I/O function and address, commands, and enable function. The tape drive moves the tape forward at normal speed due to signals from the tape drive control that are sent through the MTT control logic. The read functions read the records the same as during a read command except that no data is transferred to the I/O function for transfer to the ADP. When an IRG is detected, the EOB counter is decremented. When the count reaches zero an interrupt is generated by the tape drive control for transfer to the ADP through the I/O function. At the same time, the interrupt initiates the stop sequence. If a device command of the same speed and direction is not received within 5 ms the stop sequence is completed.

(3) *Erase forward CMD.* The FWD CMD and normal CMD cause the card cage tape drive control to send motor control signals to the tape drive through the MTT control logic. The erase CMD is received by the card cage write function. When the write function receives the ramp time complete signal from the tape drive control, it generates a time start signal to the main timing counter and energizes the erase head under control of the write control signals from the MTT control logic. After 80 ms the main timing counter sends a time signal to the address, commands, and enable function. The result is an end of erase forward signal that is sent to the card cage tape drive control. The card cage tape drive control then generates an interrupt for transfer to the ADP through the I/O function. The interrupt also initiates the stop sequence within the tape drive control. If another device command is received within 5 ms, the tape continues. If not, the stop sequence is completed. The erase time is about 80 ms. At 25 ips of tape speed, this calculates to about 9 in. of erased tape for each erase command. The erase forward CMD is used when an error is detected as a byte is written.

(4) *Erase reverse CMD*. The erase reverse CMD functions when the tape has been spaced forward to the IRG beyond the record to be erased. The command moves the tape in reverse at normal speed, and energizes the erase head. When an IRG is detected, an interrupt is generated and a stop sequence is initiated. The REV CMD and normal CMD are received by the tape drive through the MTT control logic; card cage tape drive control; address, commands, and enable function; and the I/ O function. The erase reverse CMD is received by the card cage write function. The card cage write function sends a signal over the write control lines that goes through the MTT control logic to energize the erase head in the MTT write function. The card cage write function sends the signal when the ramp time complete signal is received. With the MTT in reverse, the read heads detect the read bytes and generate the IRG time start and 1st character signals for each byte of the data record. When the 1st character signal indicates no data is present, the main timing counter sends the time signal to the tape drive control, indicating an IRG. This results in an interrupt that is sent from the tape drive control, through the I/O function, to the ADP. The interrupt initiates the stop sequence within the tape drive control. If another space reverse or erase reverse command is received within 5 ms, the tape continues. If not, it stops.

(5) *High speed forward CMD and high speed reverse CMD.* The card cage tape drive control receives the high speed forward CMD or high speed reverse CMD through the address, commands and enable and I/O functions. The motor control signals are sent to the tape drive through the MTT control logic. As the tape moves at high speed, the MTT read function detects the read bytes and the card cage read function generates a read strobe for transfer to the IRG logic in the tape drive control. The tape drive control restarts the main timing counter with a time start for each read strobe. When the IRG occurs, the read strobe and time start

signals are not generated. The time signal from the main timing counter to the tape drive control results in a request to the I/O function after 3 ms. The request is sent to the ADP. The ADP counts the requests in the alarm mode and issues an EOB when the block length field of the I/O key word in the ADP is decremented to zero. Bits 0 thru 3 of the third command byte are ignored for a high speed CMD. A stop sequence is initiated when the EOB CMD is received or at the end of tape (EOT) or beginning of tape (BOT) for forward and reverse, respectively. No interrupt is initiated for EOT or BOT. No data is transferred and error interrupts are all inhibited. The tape stops with the head positioned in an IRG.

(6) *Rewind to load point CMD.* The high speed reverse CMD is received by the tape drive through the MTT control logic; card cage tape drive control; address, commands, and enable function; and I/O function. The tape continues to move in reverse at high speed until the tape drive sensors detect the BOT reflecting strip on the tape. The BOT sensor signal is sent from the tape drive, through the MTT control, to the card cage tape drive control. The card cage tape drive control initiates an interrupt for transfer to the ADP through the I/O function. The same interrupt initiates the stop sequence within the tape drive control.

f. I/O Function. The I/O function is made up of the following subfunctions.

(1) I/O interface (para 5-1)
(2) State and byte counters (para 5-14)
(3) I/O data buffer (para 5-11)
(4) I/O strobe and request counter (para 5-13)
(5) Read, status, or interrupt output (para 5-12)

g. Test Command Generator. The test command generator is described in paragraph 5-27.

h. Front Panel. The front panel connections are described in paragraph 5-32.

i. Address, Commands, and Enable Function. This function is made up of the address, commands, and enable circuit function (para 5-15) and the MTU commands (para 5-16).

j. Card Cage Tape Drive Control Function. This function consists of the following subfunctions.

(1) Start/stop control (para 5-17)
(2) EOB counter (para 5-24)
(3) Record gap detect (para 5-23)
(4) BOT/EOT detect (para 5-26)

k. Main Timing Counter. The main timing counter is described in paragraph 5-9.

l. Error Detect. The error detect logic is described in paragraph 5-25.

m. Card Cage Write Function. This function consists of the write timing counter (para 5-18) and the write data/control (para 5-19).

n. Card Cage Read Function. This function consists of the following subfunctions.

(1) Read data (para 5-20)
(2) Read control (para 5-21)
(3) Read byte timing (para 5-22)

o. Magnetic Tape Transport (MTT). This function consists of the following subfunctions.

(1) MTT control logic (para 5-28)
(2) MTT write function (para 5-29)
(3) MTT read function (para 5-30)
(4) Tape drive (para 5-31)
(5) Front panel (para 5-32)

p. Two-Phase Clock Generator. This function is described in paragraph 5-8.

q. Power Supply. The power supply is described in paragraph 5-35.

r. MTS Interface. The MTS interface printed circuit board, when plugged in, provides a jumper for voltages and grounds. When the card is removed and the MTS umbilical cable with a card connector is plugged into the card slot, the voltage and ground connections are interrupted in the MTU and are made to the MTS. Wiring data for this function is referenced in paragraph 5-34.

5-8. Two-Phase Clock Generator (fig. 5-6). The two-phase clock generator logic is located in the card cage. The function of this logic is to provide timing for the synchronization of input/output data and command signals.

a. Clock Enable Logic. The clock enable logic provides a continuously low normal pull down/MTS disable signal (TXGN1A) during normal operation. However, when the MTU is being tested by the MTS, the MTS is connected to pin J1104-11 in order to provide ground signal TOSCEA1 to the clock enable logic. The low TOSCEA1 is inverted, thereby producing a high TXGN1A during MTS tests.

b. Clock Oscillator. A high TXGNIA prevents the output of the clock oscillator from being generated. A low TXGN1A sets the clock oscillator so that the two 16-MHz clock signals (T16MHO and T16M10) and the 4-MHz (16/4) clock signal (T04MHJ) are generated.

c. Clock Divider. The clock divider divides T04MHJ. The results are the phase one 1-MHz output signal (TXCP1A) and the phase two 1-MHz output signal (TXCP3A). The two 1-MHz signals are 180 degrees out of phase.

d. Clock Drivers. The clock drivers invert the TXCP1A and TXCP3A inputs and provide the fan out for signal drive capability. The 1-MHz PHI clock signals (TXCP1B and TXCQ1B) are 180 degrees out of phase with the 1-MHz PH2 clock signals (TXCP3B and TXCQ3B). These four clock signals are used throughout the MTU for synchronization of input and output data and command signals.

5-9. Main Timing Counter Logic (fig. 5-7). The main timing counter logic is located in the card cage. The function of the logic is to provide timed delays for start/stop and read/write/erase functions and other functions throughout the MTU. The counter counts up to 2 sec in one cycle at 1µs intervals, and does not automatically recycle.

a. Counter Restart and Main Time is Zero Logic. Any one of eight active low inputs drives the set main time count output (TCRSOB) low. The low TCRSOB sets all of the flip-flops in the main timing counter. When set, all the Q outputs are high. The eight active low inputs are as follows:

(1) 40-ms/80-ms stop delay (TSTPRA)
(2) 40-ms/150-ms start delay (TSTRRA)
(3) 50-ms flying start delay (TFSTRA)
(4) 5-ms look-ahead delay (TLADRA)
(5) First byte reset (TCRSCA)
(6) 65-ms write/80-ms erase delay (TWRGRA)
(7) 40-ms high speed gap detection delay (THSGOA)
(8) Master reset bus (TXRSOB)

Fourteen active high inputs produce the zero time output (TCZROO). The 14 active high inputs are as follows:

(1) 6µs time (TC00BQ)
(2) 10µs time (TC04BQ)
(3) 60,us time (TC10BQ)
(4) 100µs time (TC14BQ)
(5) 600µs time (TC20BQ)
(6) 1-ms time (TC24BQ)
(7) 6-ms time (TC30BQ)
(8) 10-ms-time (TC34BQ)
(9) 60-ms time (TC40BQ)
(10) 100-ms time (TC44BQ)
(11) 600-ms time (TC50BQ)
(12) 1-sec time (TC54BQ)
(13) 3-sec time (TC60BQ)
(14) 1-MHz clock enable (TC61BQ)

b. Counters Logic (fig. 5-8). The high 4-sec time input signal (TC61BQ) enables the PH2 1-MHz clock input signal (TXCP3A) for the first counter (10µs counter). The 5pis time signal (TC04BP) is active high at 5µs time, but when it goes low at 10µs, it provides the clock signal for the next counter (100OOs counter). All counters recycle and continue counting, thereby operating as a ring counter except for the last counter (4-sec counter). There are seven counters. The output of each of the first six is the clock signal for the next. The result is an overall ripple counter. The first six counters are identical and each one provides 10 outputs. In some cases, not all outputs are used. For counts one through five, the P outputs are active high, and for counts 6 through 10, the Q outputs are active high. The first six are five-stage counters that include the 10µs, 100µs, 1ms, 10-ms, 100-ms, and 1-sec counters. The seventh is a two stage counter (4-sec counter).

c. Maintime Logics (fig. 5-8). All of the maintime logic circuits work the same. A combination of inputs from one or more of the counters produces a specific output that is representative of an elapsed time from time zero. For example, the maintime-is 75µs logic in figure 5-7 produces a 1µs pulse at 75µs elapsed time. This occurs when the 1µs time (TCOOBP), 5µs time (TC04BP), 701s time (TC11BQ), and 30µs time (TC12BP) signals are all high. In the 100µs counter column of figure 5-8, row 70µs time (TC11BQ) goes high at the seventh count, which occurs at 70µs (7 x 10µs period). Row 30µs time (TC12BP) goes low at 80µs. During the 10µs period between counts seven and eight, both are high. During this period in the 10µs counter column, row 5-µs time (TC04BP) goes high at 5µs, and row 6µs time (TCOOBP) goes low at 6 µs. Between counts

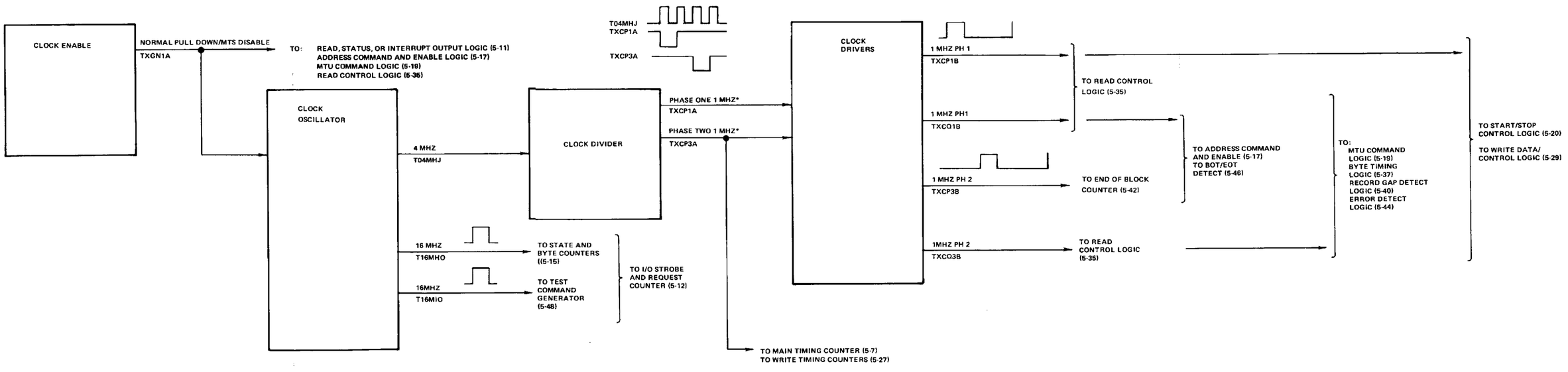


Figure 5-6. Two-Phase Clock Generator Block Diagram.

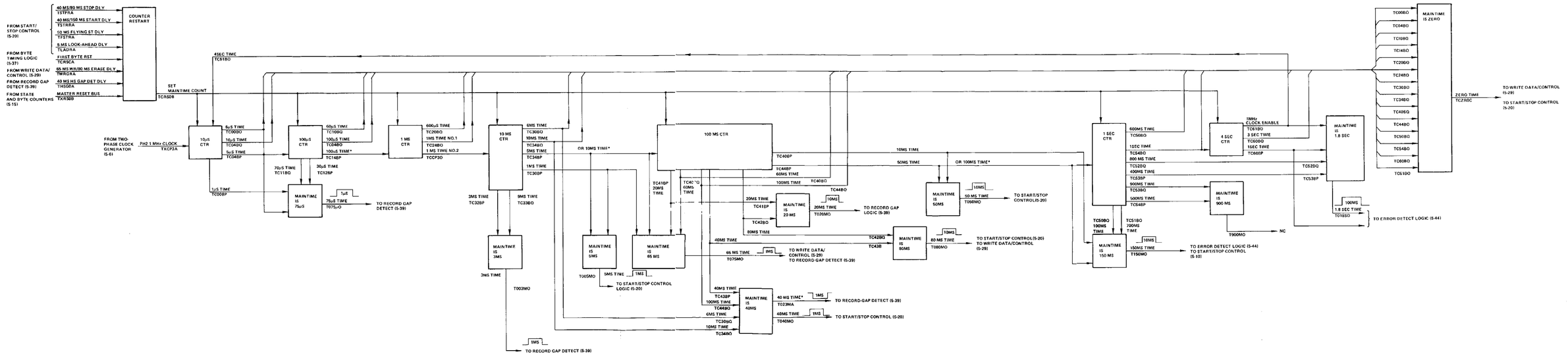


Figure 5-7. Main Timing Counter Block Diagram.

5-97/(5-98 blank)

4-SECOND COUNTER	1-SECOND COUNTER	100 MS COUNTER	10 MS COUNTER	1 MS COUNTER	100 μS COUNTER	10μS COUNTER	COUNT
1 SEC 1Hz TC54BQ	100 MS 10 Hz TC44BP	10 MS 100 Hz TC34BP	1 MS 1 KHz TC24BP	100μS 10 KHz TC14BP	10 μS 100 KHz TC04BP	1μS 1 MHZ TXCP3A	PERIOD / CLOCK
	TC50BQ	TC40BQ	TC30BQ	TC20BQ	TC10BQ	TC00BQ	TIME
	TC50BP	TC40BP	TC30BP	N/C	N/C	TC00BP	TIME*
	TC51BQ	TC41BQ	TC31BQ	TC21BQ	TC11BQ	TC01BQ	TIME
	TC51BP	TC41BP	TC31BP	N/C	N/C	N/C	TIME*
	TC52BQ	TC42BQ	TC32BQ	TC22BQ	TC12BQ	TC02BQ	TIME
	N/C	N/C	TC32BP	N/C	TC12BP	N/C	TIME*
	TC53BQ	TC43BQ	TC33BQ	TC23BQ	TC13BQ	TC03BQ	TIME
	TC53BP	TC43BP	TC33BP	N/C	N/C	N/C	TIME*
	TC54BQ	TC44BQ	TC34BQ	TC24BQ	TC14BQ	TC04BQ	TIME
	TC54BP	TC44BP	TC34BP	TC24BP	TC14BP	TC04BP	TIME*
TC60BQ							TIME
TC60BP							TIME*
TC61BQ							TIME
TC61BP							TIME*

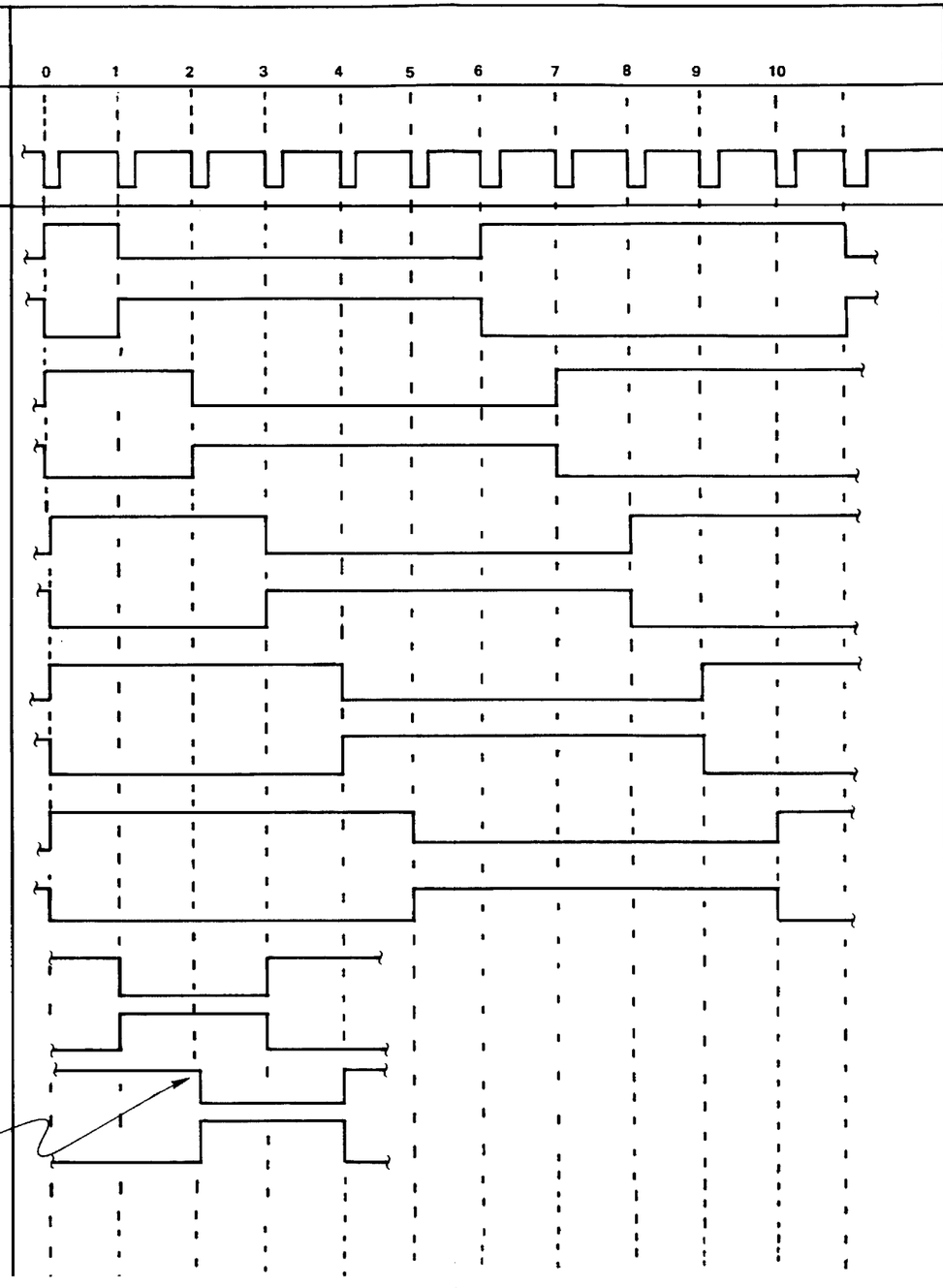


Figure 5-8. Main Timing Counter Timing Diagram.

five and six, both are high. Since all four inputs are high for 1 1us beginning at maintime is 75µs, a 1µs pulse is produced. This explanation is similar for all maintime blocks.

5-10. Input/Output Interface (fig. 5-9). The input/ output (I/O) interface logic is located in the card cage with the exception of CHANNEL SELECT switch S9. Switch S9 is located on the front panel. Switch S9 selects the channel used for the request response from the MTU to the ADP. The purpose of the I/O is to accept the command address, control code, amplifying code (eight bits of write or loop test data and the single bit parity), command (CMD), and enable inputs from the ADP. Also, the O/0 sends to the ADP the single-bit parity, indicator, and request outputs and the loop test, read, status, or interrupt data 8-bit output. The I/O consists of the ac coupled I/O, ADP or test input, I/O register, output data, and state counter start and byte counter inhibit logic functions.

a. AC. Coupled I/O. The ac coupled I/O is a bidirectional device. The interface with the ADP is over twisted-pair lines (H = high, G = low). The I/O data signal pairs (TXAOCH-TXAOCG through TXA7CH-TXA7CG) are bidirectional. The I/O data signals consist of the command address, control code, amplifying code, write data, and loop test; or the read and status data; or the interrupt data. The command signals, loop test, or write data are sent to the ac coupled I/O where they are processed to produce the active high input data signals (TXAOCT through TXA7CT) for the test input block. The loop test, read, status, or interrupt data forms the active low output data signals (TXDOOA through TXD07A). The output data is received by the ac coupled I/O from the output data block and is processed and sent to the ADP as I/O data (TXAOCH-TXAOCG through TXA7CH-TXA7CG). The bidirectional I/O parity signals (TXAPCH and TXAPCG) are the input parity for command, loop test, or write data and the output parity for read, loop test, status, or interrupt data. The I/O parity is received by the ac coupled I/O where it is processed and sent to the test input block as the active high input parity signal (TXAPCT). The active low output parity signal (TXDOPA) is received from the I/O strobe and request counter by the ac coupled I/O where it is processed and sent to the ADP as the I/O parity signals (TXAPCH and TXAPCG). The CMD signals (TXACMH and TXACMG) and the MTU enable signals (TXAENH and TXAENG) from the ADP are processed and sent to the test input block as the active high input CMD (TXACMT) and MTU enable (TXAENT) signals. The active low single bit indicator signal (TXD01A) is received by the ac coupled I/O from the output data block and is processed and sent to the ADP as the data IND signals (TXAINH and TXAING). The active low request signal (TXARQA) is received by the ac coupled I/O from the I/O strobe and request counters and is processed and sent to the ADP as the request signals (ZRQOHB and ZRQOGB). The position of CHANNEL SELECT switch S9 on the front panel determines the channel for the request output.

b. ADP or Test Input. The source of the data, command, and parity outputs depends on the selection of the test mode on the front panel. The ADP is the source in normal operation, and the test command generator is the source in test operation. The active low input data signals (TXAOCB4, TXA1CD4, TXA2CD4, TXA3CB4, TXA4CB4, TXA5CB4, TXA6CD4, and TXA7CB4) to the I/O register are a result of either the active high input data signals (TXAOCT through TXA7CT) during normal operation or the active low test data signals (TXBOCD, TXB3CD through TXB5CD, and TXB7CD) during test operation. The active low parity bit (TXAPCB4) to the I/O register is a result of either an active high input parity signal (TXAPCT) during normal operation or an active low test parity signal (TXBPCD) during test operation. The active low command bit (TXACMB4) is a result of either an active high input CMD signal (TXACMT) during normal operation or an active low test CMD signal (TXBCMD) during test operation. The active low input enable signal (TXAIEA) enables the ADP or test input block to process all signals from the ac coupled I/O. When the active low TXAIEA is present, the active high MTU enable signal (TXAENT) causes the active low MTU enable bit (TXAEND4) to be sent to the I/O register. When the ON-LINE switch S2 on the front panel is selected, the active high on-line signal (TONLNS) is sent to the ADP or test input block. This causes the new CMD and MTU enable reset I/O signal (TXARSA) to be generated. The active low TXARSA is sent to the state and byte counters when the active high input CMD signal (TXACMT) and MTU enable signal (TXAENT) are both present.

c. I/O Register. The active lows of the input data byte signals (TXAOCB4, TXA1CD4, TXA2CD4, TXA3CB4, TXA4CB4, TXA5CB4, TXA6CD4, and

TXA7CB4) set the corresponding outputs of the I/O register to an active high for the Q signals and a low for the P signals. The corresponding outputs are input data signals (TXSOBQ through TXS7BQ) and input data* signals (TXSOBP through TXS7BP). The active low parity bit signal (TXAPCB4), command bit signal (TXACMB4), and MTU enable bit signal (TXAEND4) set the corresponding Q outputs to an active high and the P outputs to a low. The corresponding output signals are parity bit (TXSPBQ), parity* (TXSPBP), CMD latch (TXSCMQ), CMD* (TXSCMP), MTU enable latch (TXSENQ), and MTU enable* (TXSENP). The eight data lines out of the I/O register that are used by the input data byte are the same lines that are used by the output data byte. The input data sets the output of the 'O register directly while the output data byte must be clocked through the I/O register to its output. The eight output data signal lines (TXDBOO through TXDB70) are active high. The active highs are clocked through the I/O register to the output data block as output data signal (TXSOBQ through TXS7BQ) by the active high I/O register output clock signal (TXXC2P). The I/O register is reset immediately after each byte is transferred by the logical combination of the high post byte reset signals (TXXA1P and TXXA2Q).

d. Output Data. The active high output data signals (TXSOBQ through TXS7BQ) are enabled by the high device inhibit signal (DEVINI) under normal conditions. However, when the MTU is tested by the MTS, DEVIN1 is low and inhibits output data. When the data is enabled by a high output strobe signal (TXXCSO), it is strobed out as the active low output data signals (TXDOOA through TXD07A) to the ac coupled I/O block. From there, the data goes to the ADP. When read data is present, the H = interrupt (INT)IL = Data enable* signal (TXDDCA) is low and the indicator signal (TXDOIA) is inhibited. When a command phase is completed, or when the output data is determined to be interrupt data by the data, status, or interrupt logic, TXDDCA goes high. When TXXCSO goes high and DEVIN1 and TXDDCA are high, the active low TXDOIA is strobed out to the ac coupled I/O block. From there, it goes to the ADP.

e. State CTR Start and Byte CTR Inhibit. With all of the P outputs of the I/O register high (no input), the state counter (CTR) start signal (TXXADA) is high. When any one of the CMD* (TXSCMP), MTU enable* (TXSENP), parity* (TXSPBP), or input data (TXSOBQ through TXS7BQ) signals goes low, TXXADA goes low and the state counter begins counting at a 16-MHz rate. The byte counter (CTR) start = H signal (TXXBCA) goes low when one of the active low master reset (TXRSOB), CMD* (TXSCMP), or MTU enable* (TXSENP) signals is present. When TXXBCA is low, the byte counter is inhibited. When all three of the inputs are high (not present), TXXBCA goes high. The high TXXBCA allows the byte counter to start counting when clocked by the recycle output of the state counter.

5-11. Input/Output Data Buffer (fig. 5-10). The input/output data buffer logic is located in the card cage. The purpose of the logic is to store the data temporarily while timed events occur. It then transfers the data when strobed by pulses that are synchronized to the MTU clock. The logic consists of two major areas; the input data register and the output data register. The input data register stores the data until transferred by the synchronized strobes to the output data register.

a. Input Data Register. The active high read data signals (TTOOBQ through TT07BQ) are available at the read data gate block when received from the read data logic. After a start delay, the read data transfer signal (TRTDOA) to the read data gate block goes low, thereby transferring the active low read output data signals (TROOCA through TR07CA) from the read data gate block to the input data register. The active low bits of the read output data byte directly set, to an active high, the corresponding loop test, write or read data outputs (TDOOBQ through TD07BQ) of the input data register. The latched data is transferred later to the output data register. The active high input loop test or write data (TXSOBQ through TXS7BQ) as well as the active high parity bit (TXSPBQ) are clocked through the input data register to produce the active high loop test, write or read data (TDOOBQ through TD07BQ) and the active high parity bit (TDOPBQ). The latched data is transferred later to the output data register. The active high clocks (TDCPOO and TDCP10) to the input data register from the input clock pulse gate block are activated by either the active low second byte write enable signal (TXEDOA) or the active low third byte loop test CMD signal (TXODOA). The input data register is reset by the active low reset outputs (TDRSOA and TDRS1A) of the reset logic block. Reset occurs when one of the following signals is sent to the reset logic block: the active low on read CMD clear for read signal (TDRSCA), the active low clear for

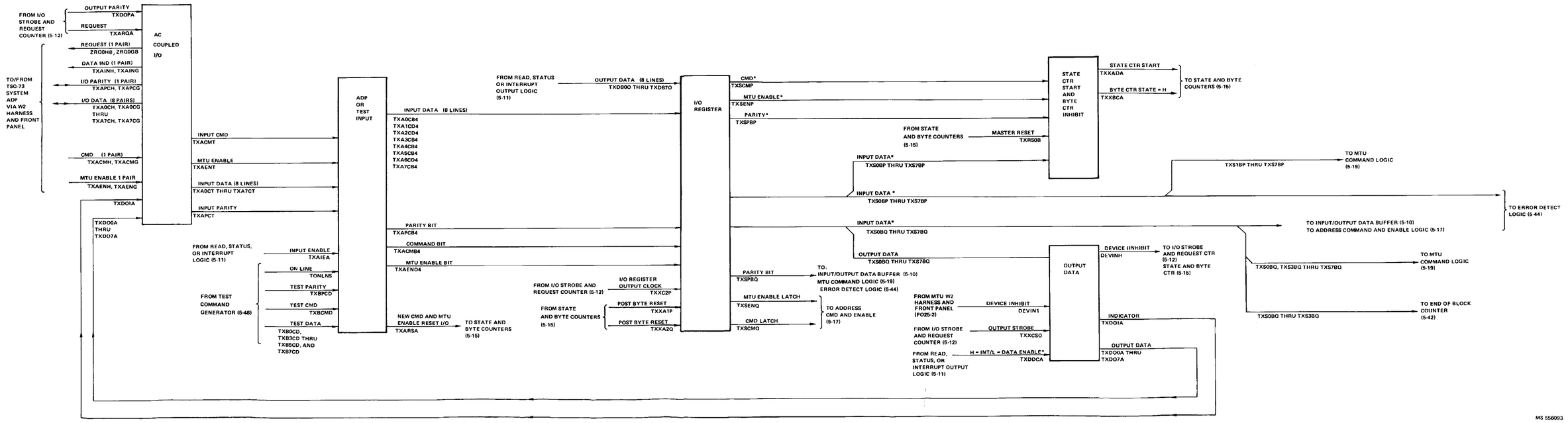


Figure 5-9. Input/Output Interface Block Diagram.

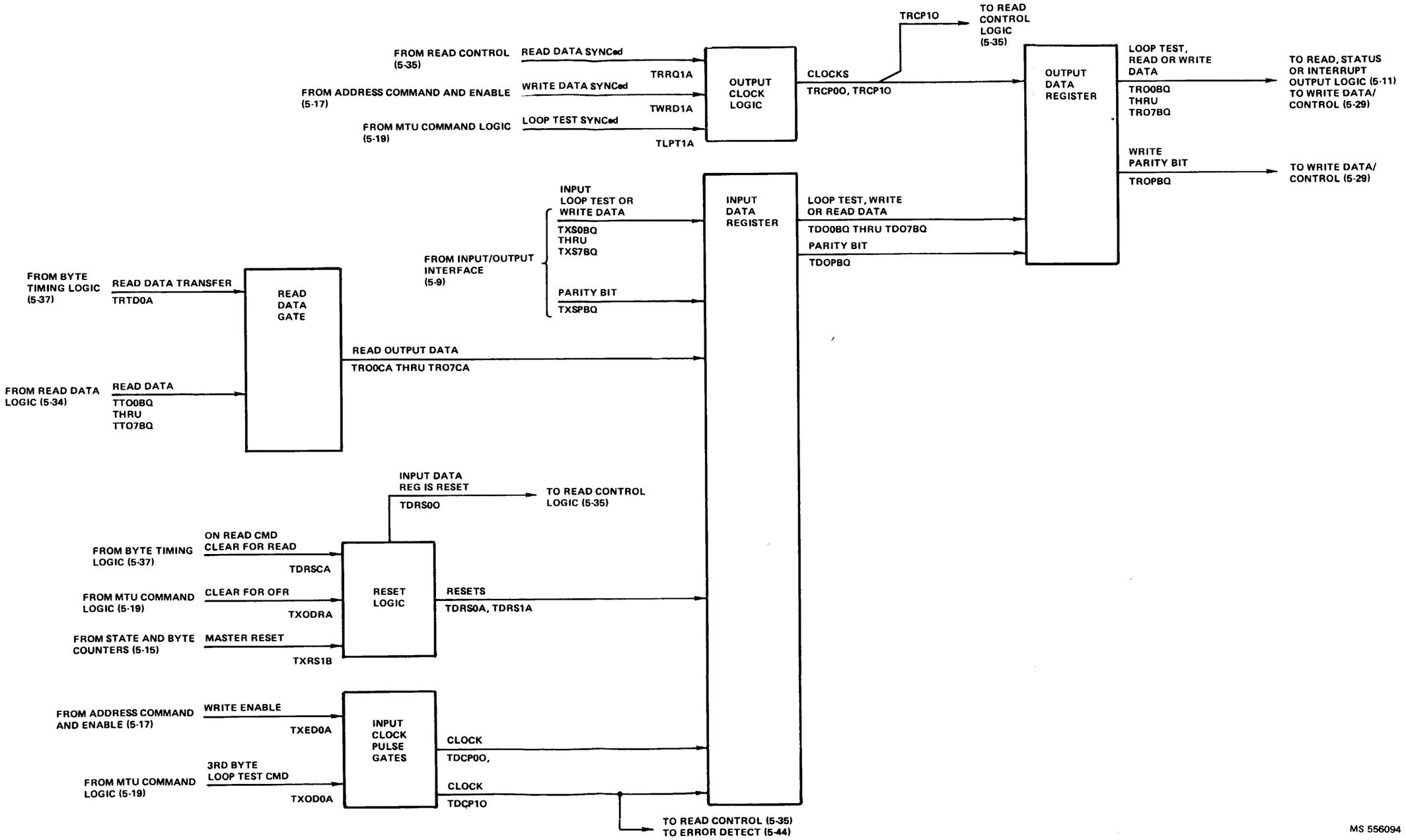


Figure 5-10. Input/Output Data Buffer Block Diagram

output from register (OFR) signal (TXODRA) when a loop test CMD occurs, or the active low *master reset* signal (TXRS1B).

b. Output Data Register. Following a read commanded start delay, the *read data synchronized* (*SYNCED*) signal (TRRQ1A) goes low. Following a write commanded delay, the *write data SYNCED* signal (TWRDIA) goes low. Following the third byte of the loop test command sequence, the *loop test SYNCED* signal (TLPT1A) goes low. A low on any one of these three inputs to the output clock logic activates the high *clocks* signals (TRCP0O and TRCP10) to the output data register. The high signal clocks the corresponding *loop test, write or read data* byte (TD00BQ through TD07BQ) through the output data register. The latched active high output is the *loop test, read or write data* (TRO0BQ through TRO7BQ). For write data, the active high *parity bit* (TDOPBQ) is clocked simultaneously with TDO0BQ through TDO7BQ. The latched output is the active high write parity bit (TROPBQ).

5-12. Read, Status, or Interrupt Output Logic (fig. 5-11). The read, status, or interrupt output logic is located in the card cage. The purpose of this logic is to determine which of the three possible types of data -- read, status, or interrupt-appear as output data. The logic also enables the input/output interface to receive inputs when none of these outputs are enabled. The read or interrupt data is available for output when enabled by the ADP following a read command or in response to an interrupt from the MTU. The status data is available for output on command of the ADP. The read latch and flip-flop (FF), interrupt latch and FF, and status FF are reset by the *master reset* signal (TXRS0B) when it goes low. When the *I/O input strobe* (TXXC4P) goes high, the low *MTS disable* signal (TXGN1A) is clocked into the three flip-flops. This effectively resets all three flip-flops. When the read flip-flop is reset, the *H= interrupt (INT)/L= read enable** signal (TXDDCA) goes high enabling the indicator output in the input/output interface logic. When the flipflops are reset and the *on line set* signal (TONLNS) is high, the *input enable* signal (TXAIEA) from the interrupt latch and FF goes high. This means that the input to the MTU from the ADP is enabled. The three main groups of logic in this function are the read output gates, the interrupt output gates, and the status output gates. The active high *read, status, or interrupt output* signals (TXDB0O through TXDB70) from the output OR gates are a result of the active low *read* signals (TXDD0A through TXDD7A), the active low *interrupt (INT)* signals (TXD10A through TXD17A), or the active low *status* signals (TXDSOA through TXDS3A, TXDS5A, and TXDS6A).

a. Read Output Gates. The active high *loop test or read data* signals (TRO0BQ through TRO7BQ), when enabled by the active high *read enable* signal (TXDDCO), are gated out as the active low *read* signals (TXDD0A through TXDD7A). Signal TXDDCO goes high when the *H= interrupt (INT)/ L = read enable** signal (TXDDCA) goes low. Signal TXDDCA goes low when the I/O is interrupt data* signal (TXXDIP) is high, and the flip-flop of the read latch and FF circuit is set. The flip-flop is set when the latch of the same circuit has been set and the *enable address* set signal (TXEA0O) goes high. The latch is set when either the *loop test synchronized (SYNCED*) (TLPT1A) or the *read request* (TREQ4A) signal goes low. When synchronized after a delay initiated by the read command, TREQ4A goes low. When synchronized after the output-from-register (OFR) command, TLPIA goes low. The OFR is the loop test command. When the latch is set, the *loop test or read wait for enable** signal (TXXDDR) goes low. The low TXXDDR results in a software busy signal in the start/stop control logic. When the flip-flop is set, the *I/O is read data** signal (TXXDDP) goes low. The low TXXDDP resets the latch within the circuit, forcing TXXDDR high. The active low *master reset* (TXRSOB) also resets the latch. The high TXXDDR deactivates the software busy signal in the start/ stop control logic.

b. Interrupt Output Gates. Bits 1 through 7 of the B-bit *interrupt (INT)* byte signals (TXDI0A through TXDI7A) represent the following input signals in bit order: *LAT/LONG parity error* (TTPERO), *no data error* (TNDATQ), *begin of tape* (TBOT0S), *end of tape* (TEOT0S), *computer data parity error* (TCDERQ), *file protect error* (TFPERQ), and *read/write IIO timing error* (TTMERQ). The B-bit TXDI7A, which would represent *MTT ready to RCV* (TRDY1O), is not used. The INT output is enabled when *INT enable* (TXXDIQ) goes high. Signal TXXDIQ goes high when the flip-flop of the interrupt latch and FF circuit is set. The flip-flop is set when the latch of the same circuit is set and the *enable ADD set* signal (TXEA0O) goes high. The latch is set when either of the *end of command interrupt* signals (TINT2A or TINT6A) goes low. When the latch is set, the *interrupt wait for enable* * signal (TXXDIR) goes low. The low TXXDIR re

sults in a software busy signal in the start/stop control logic. The latch is reset by either the low *data send inhibit* signal (TXINHR) or when the flip-flop is set by the low TXXDIP. When the latch is reset, TXXDIR goes high, deactivating the software busy signal in the start/stop control logic.

c. Status Output Gates. The first four bits of the 8-bit *status* (TXDS0A through TXDS3A) represent, in order, the following input signals; *MTT ready to RCV* (TRDY1O), *software busy* (TSBZYO), *MTC is write enabled*, and *begin of tape* (TBOT0S). The fifth bit, representing the *lateral parity error* (TLATEQ), is not used. The sixth and seventh bits represent the signals *no data error* (TNDATQ) and *end of tape* (TEOTOS). The eighth bit, representing the *longitudinal parity error* (TLNGEQ), is not used. The status output is enabled when the *status enable* signal (TXXDSQ) goes high. When the *command (CMD*) *is input to register (ITR)* signal (TXIROA) goes low, TXXDSQ goes high. The TXIR0A command is sent by the ADP when it requires the operating status of the MTU.

5-13. I/O Strobe and Request Counters (fig. 5-12). The I/O strobe and request counters logic is located in the card cage. The purpose of this logic is to provide requests for enable to the ADP. The initial requests are at the end of commands; then, when enabled, requests are sent after appropriate delays corresponding to the commands. Also, this logic provides the strobes that control the flow of input/ output data through the I/O interface to the ADP. These functions are provided by two major functional areas; the request counter and the I/O strobe counter.

a. Request Counter. A timing diagram for the request counter is provided in figure 5-13. The request counter is reset and disabled by a *low request counter (CTR) control* signal (TXXRCQ) and enabled when TXXRCQ goes high. Signal TXXRCQ is initially reset to low by the master reset signal (TXRS2B). The *master reset* signal (TXRSIB) initially resets the request counter control logic to enable *the end of command (CMD) interrupt (INT)* inputs (TINT2A or TINT6A). When TINT2A or TINT6A goes low, TXXRCQ goes high, enabling the counter and the next *16-MHz clock* signal (T16MHO). Going high starts the counter. The active low *request* signal (TXARQA) is enabled by the high *data send inhibit* (TXINHR) and the high *device inhibit* (DEVINH). Signal TXARQA goes low when the counter starts. The counter continues until the *reset request counter (RST REQ CTR)* signal (TXXR2P) goes high. At that time, it clocks in the low *MTS disable* signal (TXGN1A) which causes TXXRCQ to go low, disabling the counter. When TXARQA goes low, it disables the input to the request counter control logic. When the *enable is addressed* signal (TXEA0A) goes high, it enables the inputs. Following a corresponding delay when the *write request delay* (TWRQOA), *write start delay* (TWRQ1A), *read request delay* (TREQ4A), *Hi-speed gap delay* (THSG2A), or *loop test synchronized (SYNCED)* (TLPT1A) signals go low, TXXRCQ goes high and the counter starts. When the counter starts, the low TXARQA is generated again.

b. I/O Strobe Counter. A timing diagram for the I/O strobe counter is provided in figure 5-14. The I/O strobe counter is reset and disabled when the *I/O strobe counter control (CTR CNTRL)* signal (TXXCRO) is low and enabled when TXXCRO is high. The counter begins on the positive-going edge of the first *16-MHz clock* signal (T16MIO) after TXXCRO goes high. Initial counter reset occurs when the three input data signals--*I/O is read data** (TXXDDP), *I/O is interrupt data** (TXXDIP), and *I/O data is input to register (ITR)* (TXXDSP)--are all high (meaning no output data is enabled) and the *master reset* signal (TXRSOB) goes low. Following reset, the TXXDDP, TXXDIP, TXXDSP, *device command clock (DEV CMD CLK)* (TXDV1A), or *loop test set* (TXOD0A) signals must go low to start the counter. When either TXDV1A or TXOD0A goes low, *device (DEV) or loop test** (TXXCIP) goes low, indicating to the error detect logic that the data in the I/O interface is not output data. When the counter starts, the third positive-going edge of T16MIO clocks out the active low *output data clock* signal (TXXC2P). This signal goes to the 1/0 interface where it loads the output data into the I/O register. When TXXC2P occurs, the I/O register output of the I/O interface logic goes to the error detect logic where the *output parity (PAR) check odd =L, even =H* signal (TPS60A) is generated. The *device inhibit* signal (DEVINH) from the I/O interface is held high in order to enable the I/O strobe counter. When TPS60A is high and the *output strobe* (TXXCSO) goes high, the active low *odd = H even = L output parity* signal (TXDOPA) is sent through the ac coupled I/O0 of the I/O interface logic to the ADP. Signal TXDOPA goes high when TPS60A goes low; however, when the *output strobe* signal (TXXCSO) occurs, TXDOPA remains low.

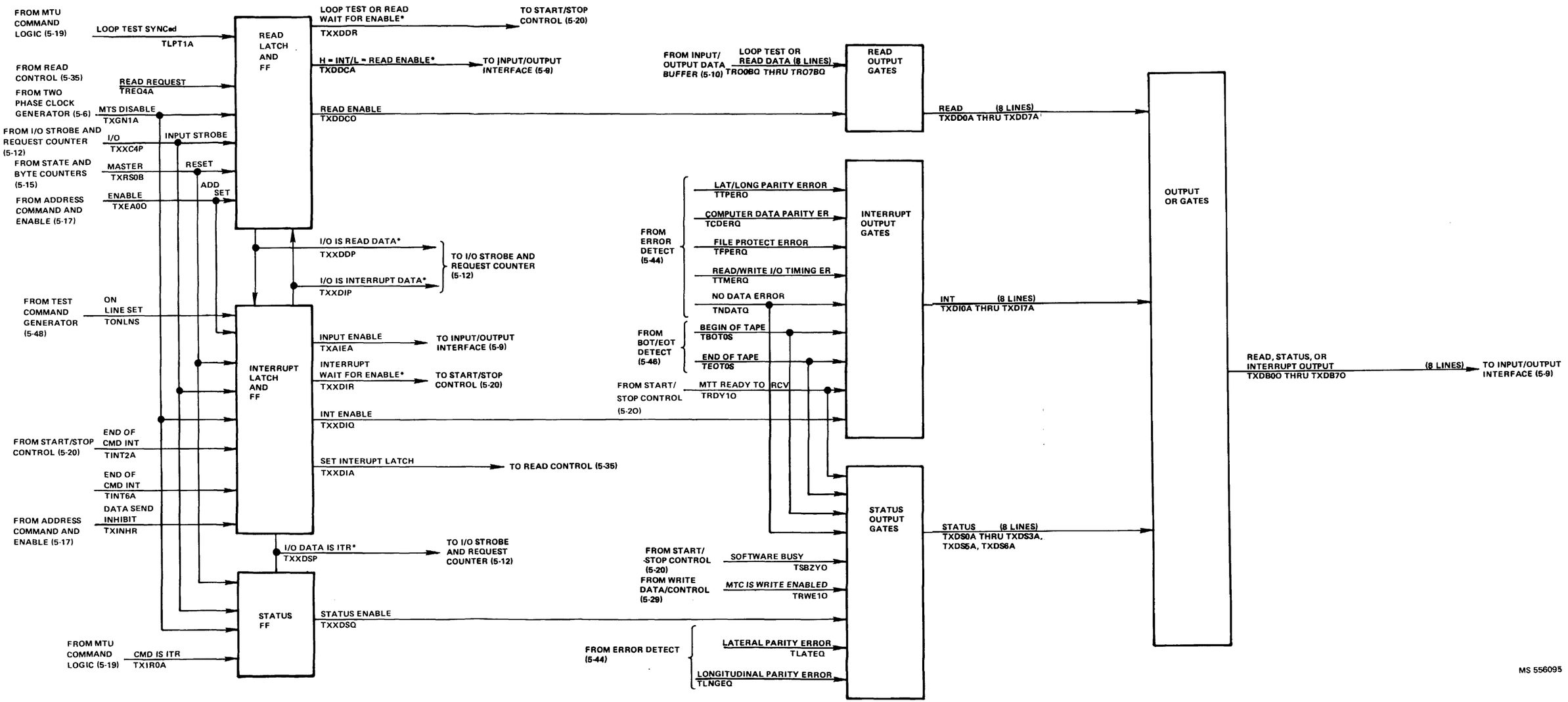


Figure 5-11. Read, Status, or Interrupt Output Block Diagram

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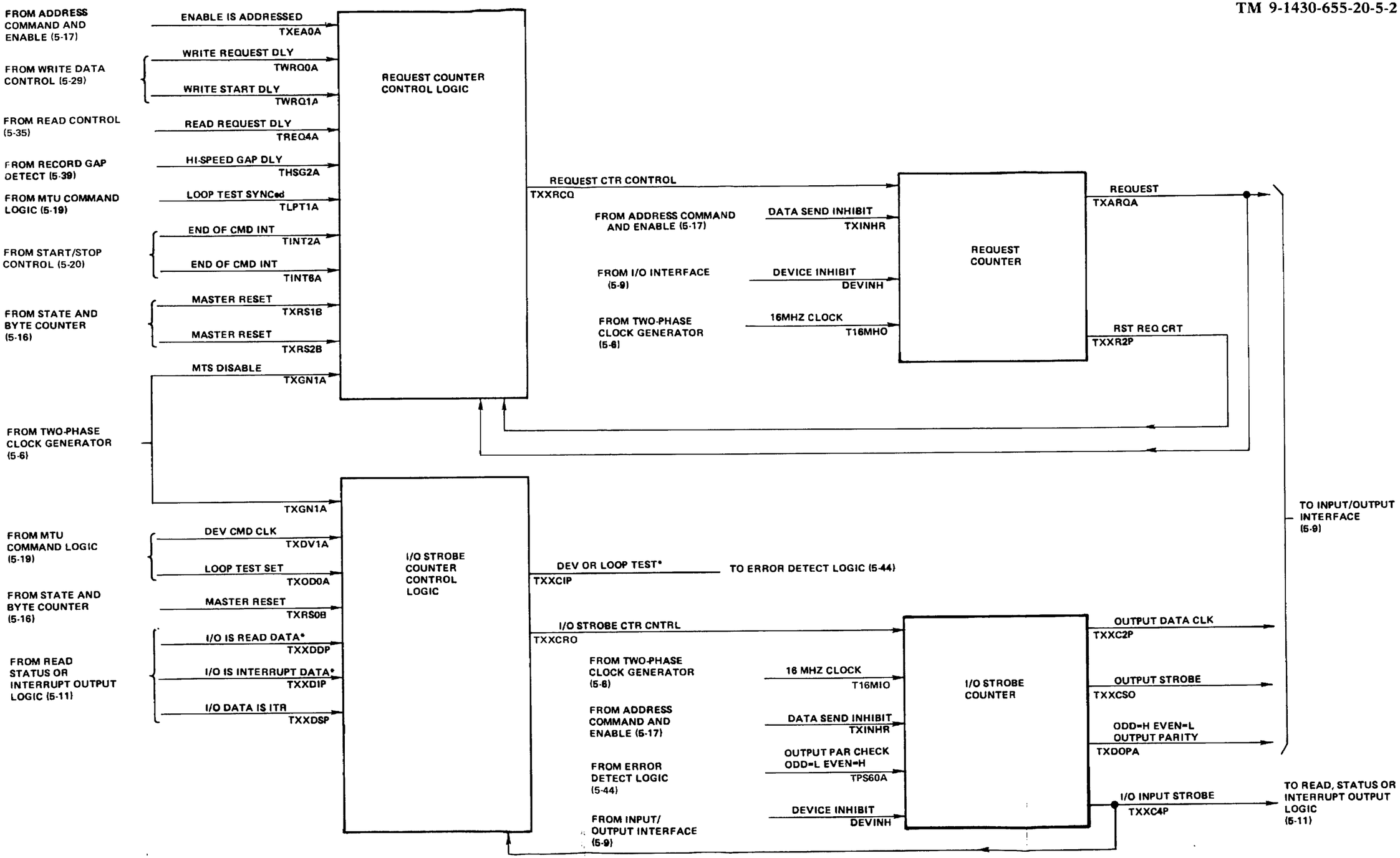

Figure 5-12. I/O Strobe and Request Counters Block Diagram

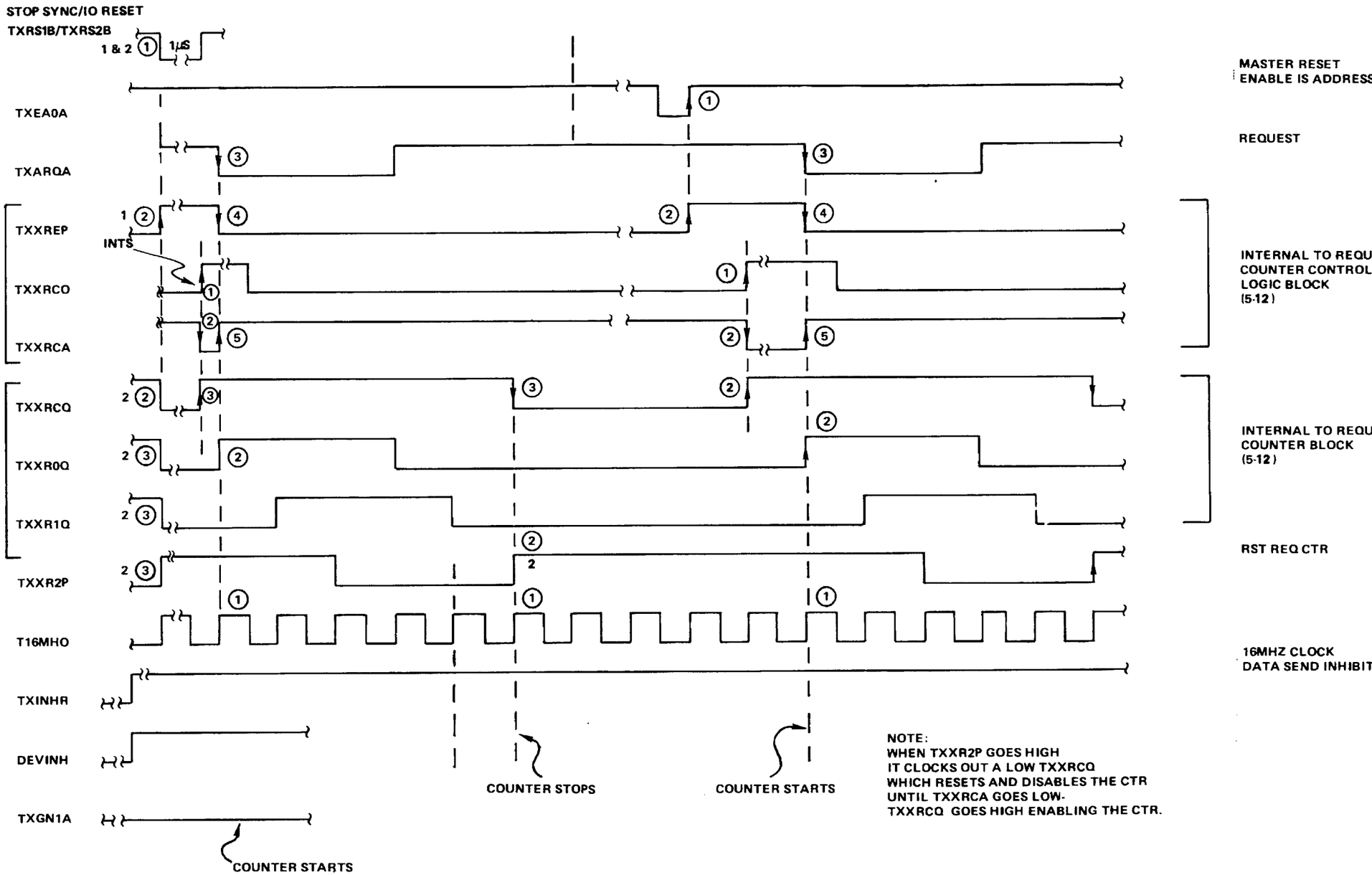

Figure 5-13. Request Counter Timing Diagram

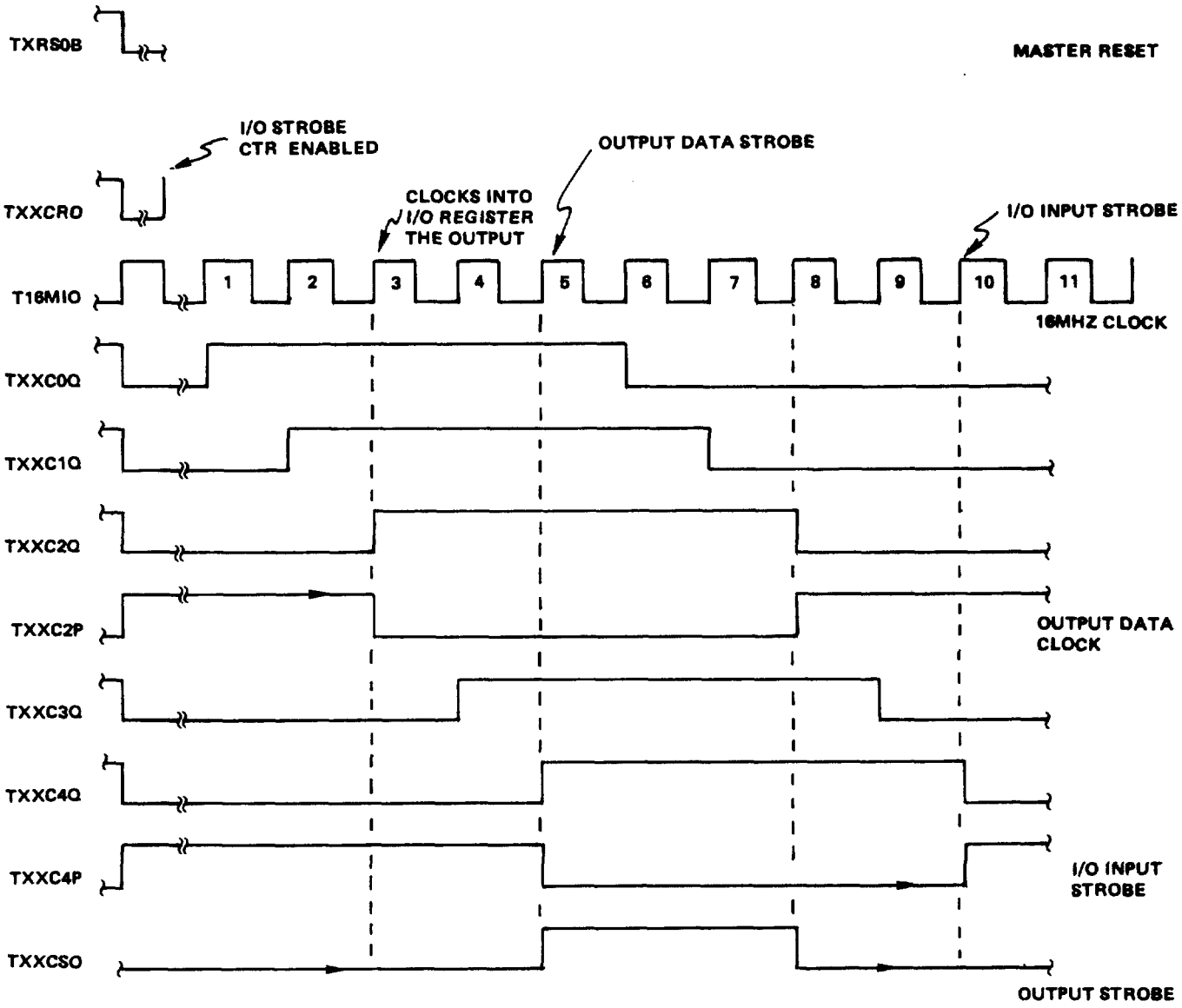

Figure 5-14. I/O Strobe Counter Timing Diagram

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The active high TXXCSO is enabled by the high data send inhibit signal (TXINHR). The fifth positive-going edge of T16MIO clocks out TXXCSO. This signal goes to the input/output interface where it strobes the output data through the ac coupled I/O to the data lines going to the ADP. The tenth positive-going edge of T16MIO clocks out the active high I/O input strobe signal (TXXC4P). Signal TXXC4P goes to the I/O strobe counter control where it clocks in the low TXGN1A. Signal TXXC4P also goes to the read, status, or interrupt output logic where it results in the high TXXDDP, TXXDIP, and TXXDSP. These high signals, along with the low TXGN1A, result in a low TXXCRO that resets the I/O strobe counter. Signal TXXC4P to the read, status, or interrupt logic also causes an input enable signal to be generated. The input enable signal enables data to be transmitted from the ADP and through the I/O register of the I/O interface.

5-14. State and Byte Counters (fig. 5-15 and 5-16). The state and byte counters logic is located in the card cage. The purpose of the logic is to identify the three command states and to provide timing to the I/O interface; address, commands, and enable logic; and error detect logic. The state and byte counters work together to perform this function. The counters are reset and remain disabled when the command and enable signals or a stop command occurs. The byte counter is also reset when either the command or the enable occurs (for example, when data is transferred to or from the ADP). A MTU enable occurs for each read or write data byte transferred; therefore, the state counter cycles through for each byte. When there is no data present, the state counter completes one cycle, resets, and remains disabled. The state counter is enabled and starts counting when any input from the ADP or any output from the MTU is present on the output lines of the 1/O register in the I/O interface logic. The byte counter is enabled when there is no command, enable, or master reset present. The byte counter increments when clocked at the end of each complete cycle of the state counter. The byte counter logic includes the set/ reset drivers, state counter control, state counter, and byte counter. The three command states are represented by bytes one, two, and three, respectively. During the first byte, with the appropriate single bit command or enable, the address bit from the ADP is received on one of the data lines to the MTU. During the second byte, the command on the data lines is received and decoded by the MTU to the specific type of command. During the third byte, the specific type of command on the data lines requiring a clock is transferred within the MTU to the appropriate actuating logic.

a. Set/Reset Drivers. The set/reset drivers logic works as an OR gate. When the *stop synchronizer (SYNC)* (TXST1A), *device inhibit* (DEVINH), or *new command (CMD) and MTU enable reset I/O* (TXARSA) signals go low, the *master reset* signals (TXRS0B, TXRSIB, and TXRS2B) go low. The three identical active low signals provide the needed fan out to reset the various logic circuits throughout the MTU.

b. State Counter Control. The state counter control logic resets and disables the state counter when the *master reset* signal (TXRS2B) goes low or when the *byte counter clock* signal (TXXA3P) goes high. It does this by sending a low *state counter reset and enable* (*ST CTR RST and EN)* signal (TXXACP) to the state counter. When any signal appears on the output lines of the I/O register in the I/O interface, the *state counter start = L* signal (TXXADA) goes low. This causes TXXACP to go high and the state counter to start.

c. State Counter. When the *master reset* signal TXRS2B goes low, it sets the *I/O register post byte reset* signal (TXXA2Q) high and (allowing for the propagation delay through the state counter control) TXXACP goes low and resets the state counter. All Q outputs go low and P outputs go high when reset. See figure 5-16 for state counter output levels when clocked by the *16-MHz clock* signal (T16MHO) after being enabled by the high TXXACP.

d. Byte Counter. The byte counter is reset by the *byte counter start = H*, *reset (RST)=L* signal (TXXBCA) whenever there is a command or enable input or when the master reset occurs. When TXXBCA goes high, the counter is enabled and the counter increments each time the *byte counter clock* signal (TXXA3P) goes high. See figure 5-16 for counter output levels (for example, when TXXBOP, TXXB1P, TXXAOQ, and TXXA3Q are high, the *command (CMD) and enable (EN) latch reset* signal (TXX04A) goes low).

5-15. Address, Command, and Enable Logic (fig. 5-17). The address, command, and enable logic is located in the card cage with the exception of CHANNEL SELECT switch S9, which is on the

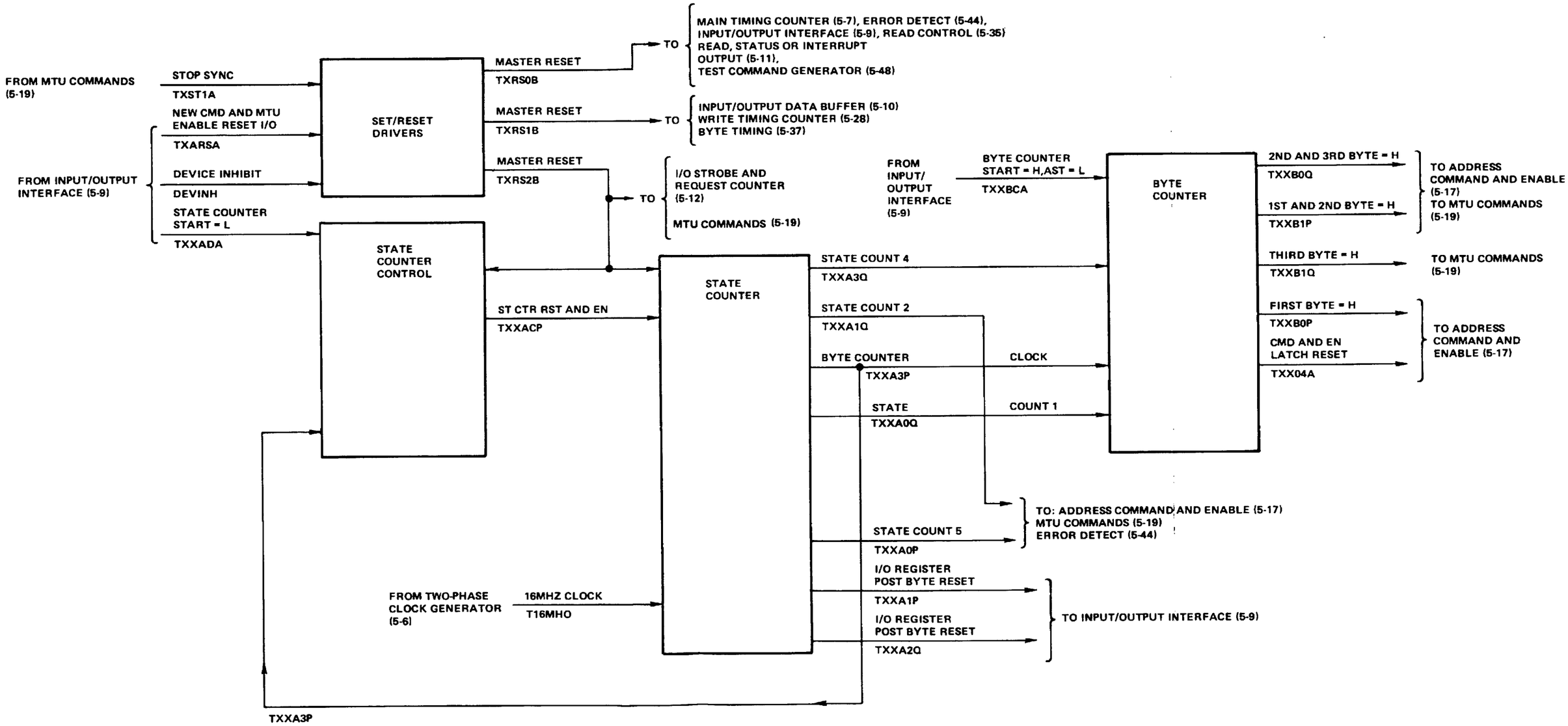
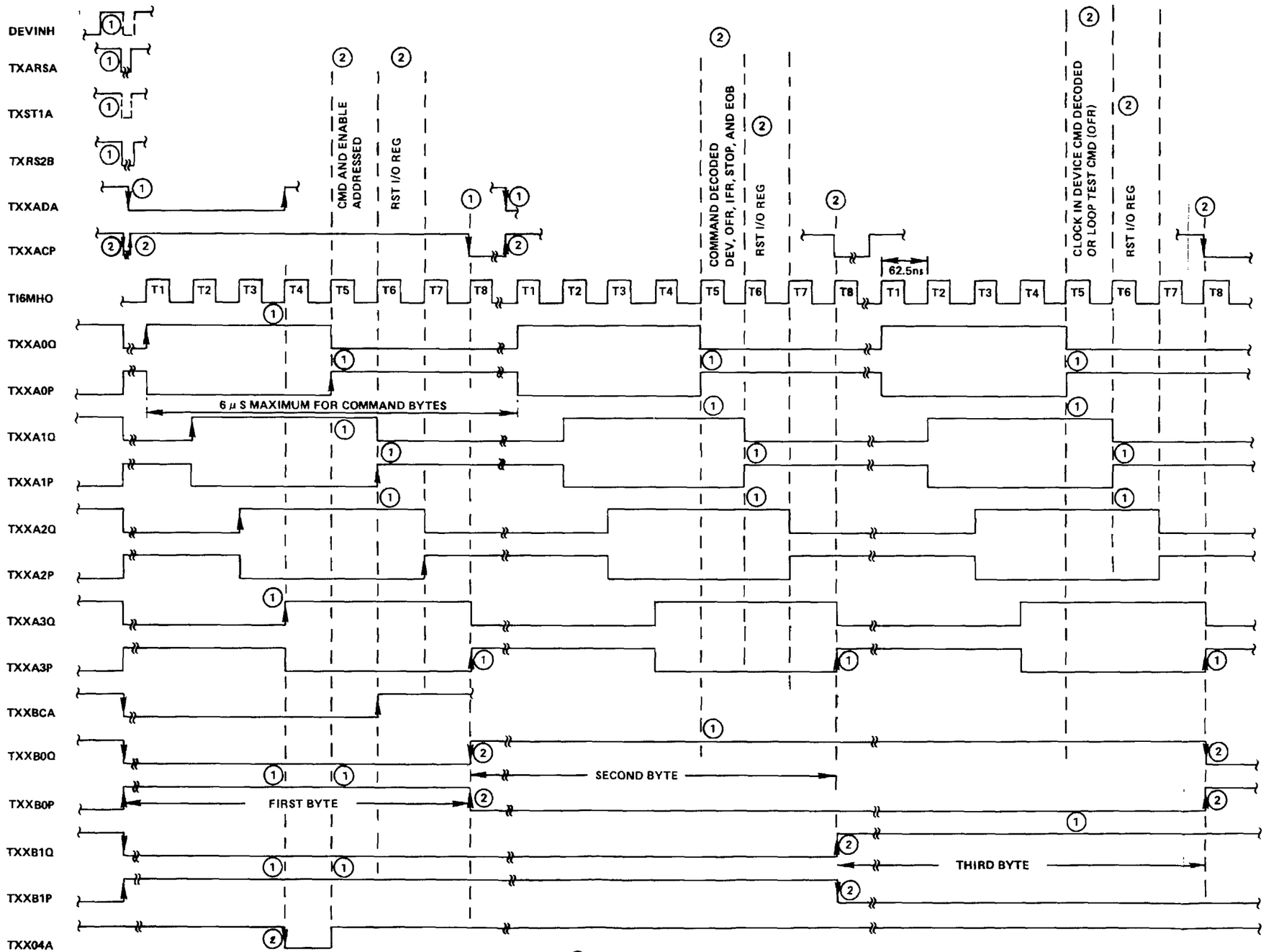


Figure 5-15. State and Byte Counters Block Diagram



VICE INHIBIT (VOLTAGE NOT INHIBITED BY MTS = HIGH)

W CMD AND MTU ENABLE RESET I/O

OP SYNC

ISTER RESET

STATE COUNTER START = L

ST CTR RST AND EN

16 MHZ CLOCK

STATE COUNT 1

STATE COUNT 5

STATE COUNT 2

STATE COUNT 6/ I/O REGISTER POST BYTE RESET

STATE COUNT 3/ I/O REGISTER POST BYTE RESET

STATE COUNT 7

STATE COUNT 4

STATE COUNT 8/BYTE COUNTER CLOCK

BYTE COUNTER START = H, RST = L

BYTE COUNT 1/ 1ST AND 2ND BYTE = H

BYTE COUNT 3/ FIRST BYTE = H

BYTE COUNT 2/ THIRD BYTE = H

BYTE COUNT 4/ 1ST AND 2ND BYTE = H

CMD AND EN LATCH RESET

NOTE: (1) INDICATES THE CONDITIONAL AND/OR ACTUATING LOGIC LEVELS.
(2) INDICATES THE RESULT AND LOGIC LEVELS.

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Figure 5-16. State and Byte Counters Timing Diagram

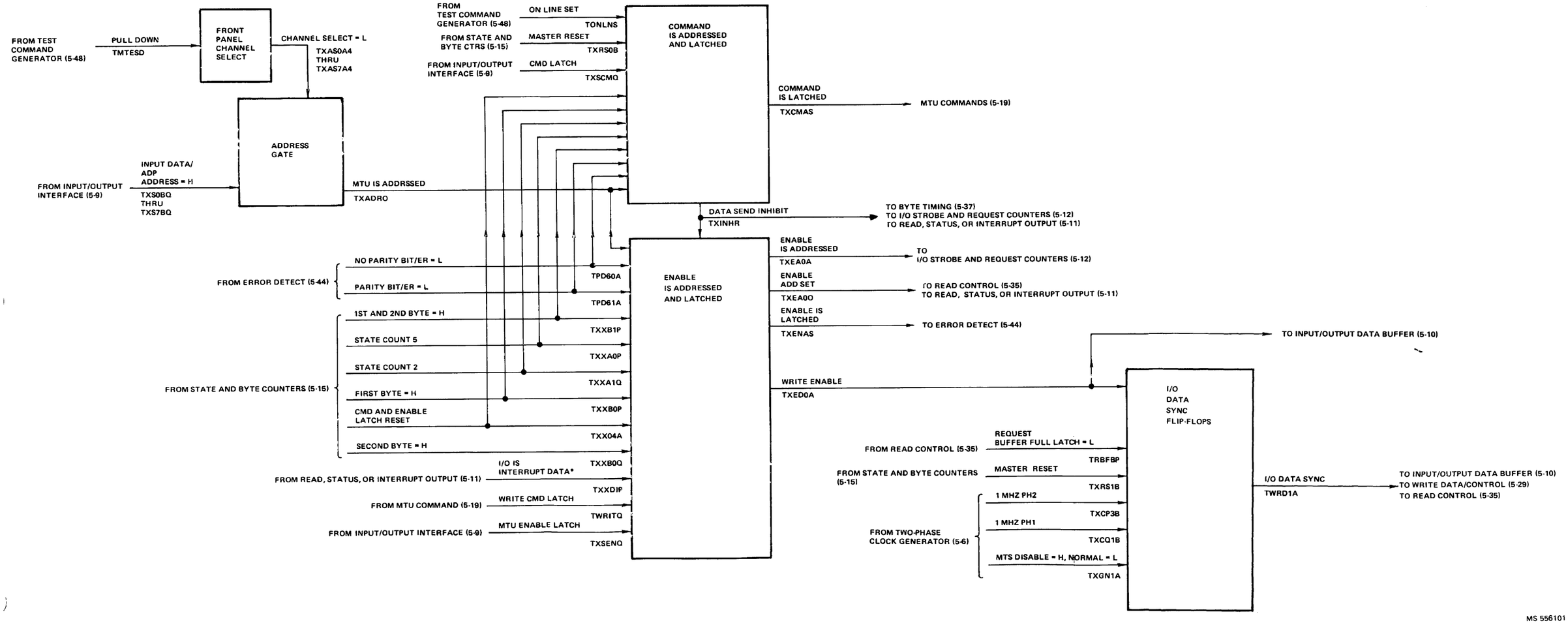

Figure 5-17. Address Command and Enable Block Diagram

front panel. The purpose of this logic is to identify the MTU to the ADP while being addressed by the ADP with a command and/or an enable signal. Also, this logic synchronizes I/O write data with the MTU clock. The major logic functions are as follows: front panel channel select, address gate, command is addressed and latched, enable is addressed and latched, and I/O data synchronizer (SYNC) flip-flops.

a. Front Panel Channel Select and Address Gate. Pulldown signal (TMTESD) is always low and is applied to the center contact of CHANNEL SELECT switch S9 on the front panel. The low is applied through the center contact to one of eight output contacts and thereby becomes one of the *channel select=L* signals (TXAS0A4 through TXAS7A4). The switch position determines which line is low. Signals TXAS0A4 through TXAS7A4 are applied to the address gate. The low input enables one of the address gates. If one of the *input data/ ADP address*=H signals (TXS0BQ through TXS7BQ) is high to the enabled gate, the *MTU is addressed*=H signal (TXADRO) goes high. Signal TXADRO is applied to both the command and enable blocks.

b. Command is Addressed and Latched, Enable is Addressed and Latched. The latches are set when the following conditions are fulfilled: timing from the state and byte counters is present; there are no I/O data errors from the error detect logic; proper command and/or enable signals are sent from the ADP and through the input/output interface; and proper addressing is received from the ADP through the address gate. The conditions are met when all the input signals representing the conditions go high. The timing signals *1st and 2nd byte=H* (TXXB1P), *state count 5* (TXXA0P), *state count 2* (TXXA1Q), and *first byte =H* (TXXB0P) go high during the first byte of the command phase (fig. 5-16). The same timing signals also go high during the first byte that occurs for each enable when data is transferred to or from the ADP. The error signals *no parity bit/ER=L* (TPD60A) and *parity bit/ER=L* (TPD61A) are high to the command and enable functions if the error detect logic detects no errors on the output lines of the I/O register in the I/O interface. The *MTU is addressed = H* signal (TXADRO) to both the command and enable functions is high when the MTU is addressed. The *command (CMD) and enable latch reset* signal (TXX04A) resets both latches immediately prior to the time for setting the latch. Both latches are also reset by TXXB1P when it goes low at the end of the second byte (fig. 5-16). The high *command (CMD) latch* (TXSCMQ) and *MTU enable latch* (TXSENQ) signals are applied to their respective logic functions when a command or enable is received from the ADP.

(1) *Command is addressed and latched*. The high signals *1st and 2nd byte=H* (TXXB1P), *state count 5* (TXXA0P), *state count 2* (TXXA1Q), *first byte=H* (TXXB0P), *no parity bit/erase(ER)=L* (TPD60A), *parity bit/ER=L* (TPD61A), and *command (CMD) latch* (TXSCMQ) set the command latch. When set, *the command is latched* output (TXCMAS) goes high. Signal TXCMAS goes low when reset. The latch is reset by the low TXXB1P or *command (CMD) and enable latch reset* signal (TXX04A) (fig. 5-16) and by the master reset signal (TXRS0B) when it goes low. The other output of this logic function is the *data send inhibit* signal (TXINHR). Signal TXINHR is latched high when TXCMAS goes high and both TXRS0B and the *on-line set* signal (TONLNS) are high. When TXINHR is high, it permits transfer of data by enabling the I/O strobe and request outputs of the I/O strobe and request counter logic. A low TXRS0B or TONLNS sets TXINHR low. A low TXINHR resets the enable latch.

(2) *Enable is addressed and latched*. The signals *1st and 2nd byte = H* (TXXB1P), *state count 5* (TXXA0P), *state count 2* (TXXA1Q), *first byte =H* (TXXB0P), *no parity bit/ER = L* (TPD60A), *parity bit/ER = L* (TPD61A), and *MTU enable latch* (TXSENQ) must be high to set the latch. When this occurs, in addition to setting the *enable is latched* signal (TXENAS) high, the *enable is addressed* signal (TXEA0A) is low and the *enable add set* signal (TXEA0O) is high. The latch is reset by the low TXXB1P or TXX04A (fig. 5-16). The latch is also reset by the *low I/O is interrupt data** signal (TXXDIP) and the low *data send inhibit* signal (TXINHR) from the command is addressed and latched block. When reset, the *enable is latched* signal (TXENAS) goes low. The other output of this logic function is the active low *write enable* signal (TXED0A). The *write CMD latch* signal (TWRITQ) goes high during the third byte of the command phase. Signal TXENAS goes high during the first byte of the data phase when the enable is addressed. During the second byte of the data phase, the state and byte counter signals *second byte=H* (TXXB0Q), *state count 5* (TXXA0P), and *state count 2* (TXXA1Q) go high (fig. 5-16). With TWRITQ,

TXXB0Q, TXXA0P, and TXXA1Q high, TXED0A goes low. Signal TXED0A is used as a clock for the input data register of the input/output data buffer and it is used to set the first flip-flop of the I/O data SYNC flip-flops logic function.

c. I/O Data SYNC Flip-Flops. A timing diagram for the I/O data synchronizer (SYNC) flip-flops is provided in figure 5-18. The input write data from the input/output data buffer is synchronized to the *1-MHz PH2 clock* signal (TXCP3B) by the *I/O data SYNC* signal (TWRD1A). Signal TWRD1A is the clock for the output register of the buffer. If the request buffer of the read control logic is full, the *request buffer full latch=L* signal (TRBFBP) goes low. When TRBFBP is low, TWRD1A does not go low, and write data is not clocked out of the output register of the input/output data buffer.

5-16. MTU Commands Logic (fig. 5-19). The MTU commands logic is located in the card cage. The purpose of this logic function is to decode all of the commands from the ADP for use in the MTU. The commands are as follows:

Device command (DEV CMD)
Output from register command (OFR CMD)
Input from register command (IFR CMD)
Stop command (stop CMD)
End of block command (EOB CMD)

a. Device Commands (fig. 5-16 and 5-19). The device commands are received during the three bytes of the command phase. During the first byte, the MTU is addressed. During the second byte, the device commands are received. During the third byte, the amplifying command is received. The device commands control the operation of the magnetic tape - transport and the reading and writing of data on the tape. The device commands logic consists of the device command (CMD) decoder and latch, valid new device CMD logic, end-of-erase forward (FWD) CMD gate, and the following flip-flops.

Rewind flip-flop (FF) with decoder
Direction flip-flop (FF)
New speed flip-flop (FF)
Erase forward flip-flop (FF) with decoder
Space record flip-flop (FF) with decoder
Read flip-flop (FF) with decoder
Write flip-flop (FF) with decoder
Hi speed flip-flop (FF) with decoder
Erase reverse flip-flop (FF) with decoder

(1) *Device CMD decoder and latch*. All the inputs to the device CMD decoder and latch must be high. The *CMD is latched* signal (TXCMAS) goes high during the first byte, indicating that the MTU has been addressed. During the second byte, the *second byte = H* (TXXB0Q), *state count 5* (TXXA0P), and *state count 2* (TXXA1Q) signals go high. The data lines TXS0BQ, TXS1BP, TXS2BP, and TXS3BQ) are high inputs during the second byte if the device command is active. The *hardware busy = L* signal (TBUSYR) is reset high by the master reset when the *no data/rewind (REW)=H* signal (TXDVCO) is high and no data is present during the second byte. Observe that only two data lines TXS0BQ and TXS3BQ represent logic ones when there is no data; therefore, the odd *parity* bit (TXSPBQ) must be high. When TXXA0P goes high, the latch is set and the *DEV CMD Reset (RST)* output signal (TXDEVR) goes low. With the *1st and 2nd byte=H* signal (TXXB1P) high when the *DEV CMD SET* signal (TXDEVS) goes high, *the reset end of block counter (RST EOB CTR*) output signal (TEBRSA) goes low. At the end of the third byte, the *2nd and 3rd byte = H* signal (TXXB0Q) goes low, resetting TXDEVR to high and TXDEVS to low.

(2) *Valid new device CMD logic.* One of the decoded device command signals must be low to indicate that an amplifying device command has been received during the third byte. The decoded device command signals are:

No data/rewind (REW)=L (TXDVCA)
Space record (SPA REC)=L (TSPA1A)
Erase forward (ERS FWD)=L (TESF1A)
Erase reverse (ERS REV=L (TESR11A)
High speed (HI SP)=L (THSP1A)
Read=L (TRED11A)
Write=L (TWRT1A)

The *parity bit/error(ER)=L* (TPD61A) and *no parity bit/error(ER)=L* (TPD60A) signals must be high to indicate no parity errors for the third byte. The *third byte = H* signal (TXXB1Q) and the *state count 2* signal (TXXA1Q) must be high. With these conditions satisfied, when the *state count 5* signal (TXXA0P) goes high, the *DEV CMD* clock (CLK) output signal (TXDV1B) goes high and the *DEV CMD CLK** output signal (TXCV1A) goes low.

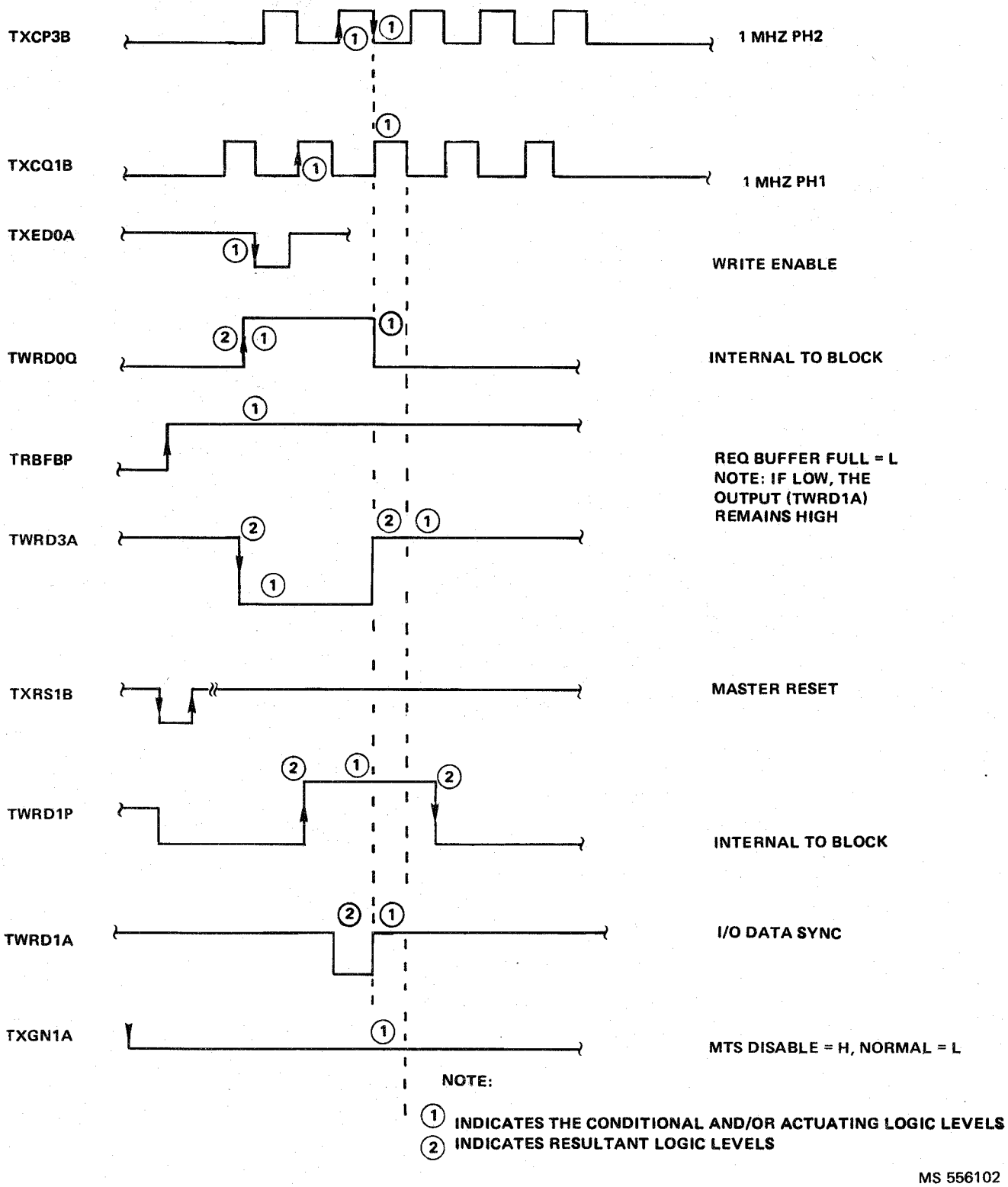

Figure 5-18. I/O Data SYNC Flip-Flops Timing Diagram

(3) *Amplifying device commands*. The nine flip-flops representing the amplifying commands work in a similar manner. The flip-flops are all reset by the master reset signals except for the write FF with decoder; it resets when the output from register (OFR) CMD decoder and latch is set by the *OFR set** signal (TXODRA). The OFR CMD decoder provides for a loop test of the input and output circuits of the MTU. Each of the flip-flops may receive a coded amplifying device command during the third byte. Code reception is indicated by a low decoded device command signal. These signals also go to the valid new device CMD logic function. The high *DEV CMD CLK* signal (TXDV1B) is applied to each flip-flop during the third byte of the command phase. The decoded device command is clocked through the applicable flip-flop by TXDV1B, forcing its Q output high and its P output low. The amplifying device command flip-flops function is described in the following subparagraphs.

(a) Read FF with decoder. When the *read command* signals (TXS4BQ, TXS5BQ, TXS6BP, and TXS7BP) are high, the *read=L* signal (TRED1A) goes low. The low TRED1A is inverted and then clocked into the read FF by TXDV1B. The flop-flop produces the *read= H* output signal (TREADQ) and the low *no read=H* output signal (TREADP). The flip-flop is reset by the master reset signal (TXRS2B).

(b) Write FF with decoder. When the *write command* signals (TXS4BQ, TXS5BQ, TXS6BQ, and TXS7BQ) are high, the *write=L* signal (TWRTLA) goes low. The low TWRT1A is inverted and then clocked into the write FF by TXDV1B which produces the *write=H* (TWRITQ) and *no write = H* (TWRITP) output signals. The flip-flop is reset by the low *OFR set** signal (TXODRA).

(c) High speed FF with decoder. When the high speed command signals (TXS5BQ, TXS6BP, and TXS7BQ) are high, the *high speed (HI SP)= L* signal (THSP1A) is low. The low THSP1A is inverted and then clocked into the HI speed FF by TXDV1B. This causes the HI speed FF to produce the *HI SP = H* (THISPQ) and the low *low speed (LO SP)=H* (THISPP) output signals. With THISPQ high and the *synchronized end of block command (SYNCHED EOB CMD)* signal (TXEB1Q) high, the next *1-MHz PH2* clock (TXCP3B) clocks out the *high speed end of block command (HI-SP EOB CMD)* signal (THSC1A). The HI speed FF is reset by the *master reset* signal (TXRS2B).

(d) Erase reverse FF with decoder. When the *erase reverse* command signals (TXS4BP, TXS5BP, TXS6BQ, and TXS7BQ) are high, the *erase reverse (ERS REV) =L* signal (TESR1A) is low. The low TESR1A is inverted and then clocked by TXDV1B into the erase reverse FF. This causes the reverse FF to produce the *ERS REV latch = L* output signal (TERSRP). A low TESR1A, *No Read=H* (TREADP), or *no write=H* (TWRITP) signal produces the high *read, write, or erase reverse (R, W, or ERS REV)=H* signal (TGAP1O).

(e) Rewind FF with decoder. When the *rewind command* signals (TXS4BP, TXS5BP, TXS6BP, and TXS7BP) are high, the *no data/rewind (REW)=L* signal (TXDVCA) is low. The low TXDVCA is inverted to produce the *no data/REW=H* signal (TXDVCO). Signal TXDVCO is clocked into the rewind FF by TXDV1B. This causes the rewind FF to produce the *rewind (REW) latch=L* output signal (TREWDP). The flip-flop is reset by the *master reset* signal (TXRS2B).

(f) Direction FF. When TXDV1B goes high, if the *reverse (REV) = H/forward (FWD) = L* signal (TXS4BP) is low, the *forward (FWD)=H* output signal (TDIRSQ) goes high. If TXS4BP is high, then the *reverse (REV)= H* output signal (TDIRSP) goes high.

(g) New speed FF. If either the *rewind (REW)=L* (TXDVCA) or the *high speed (HI SP)=L* (THSP1A) signal is low when TXDV1B goes high, the *HI SP=H* output signal (TSPNSQ) goes high. If both input signals are high, the *low speed (LOW SP)=H* signal (TSPNSP) goes high. The output signals are actuated by the TXDV1B clock.

(h) Erase forward FF with decoder. When the *erase forward* command signals (TXS4BQ, TXS5BP, TXS6BQ, and TXS7BP) are high, the *erase forward (ERS FWD)= L* signal (TESF1A) goes low. The low TESF1A is inverted and clocked into the flip-flop by TXDV1B. The flip-flop produces the ERS FWD=H output signal (TERSFQ). The flip-flop is reset by the *master reset* signal (TXRS2B). While reset, the flip-flop produces the *no ERS FWD =H* signal (TERSFP).

(i) Space record FF with decoder. When the *space record command* signals (TXSSBP, TXS6BP, and TXS7BQ) are high, the *space record (SPA REC)=L* signal (TSPA1A) is low. Signal TSPA1A is inverted to produce the *stop/SPA REC=H* signal (TSPA10). The high TSPA10 output signal is also clocked into the space record FF to produce the *SPA REC latch=H* output signal (TSPACQ).

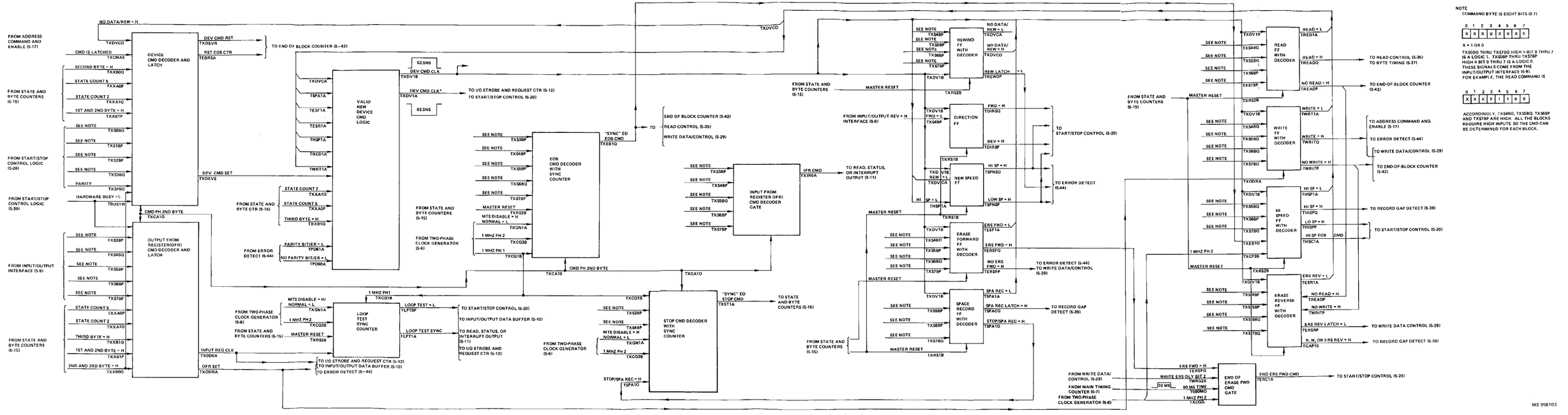

Figure 5-19. MTU Commands Block Diagram

(j) End of erase forward command (FWD CMD) gate. When the command is erase forward, the *erase forward (ERS FWD)= H* signal (TERSFQ) is active. Eighty ms after the start delay for the erase function, the *write/ERS delay (DLY) bit 2* signal (TWRG2S) is set high. The *80-ms time* signal (T080)MO) goes high at this time and remains high for 10 ms. The next *1-MHz PH2* clock (TXCQ3B) clocks out the *low end erase forward command (end ERS FWD CMD)* signal (TERC1A).

b. OFR CMD (fig. 5-16 and 5-19). For the MTU, the OFR CMD is a test of the input/output circuits. The OFR CMD is called the loop test because the third byte of the command is looped through the I/O interface; input/output data buffer; read, status, or interrupt logic; and back through the I/O interface to the ADP. This function is represented by the OFR CMD decoder and latch and the loop test SYNC counter. The OFR CMD decoder and latch function decodes -the second byte of the OFR CMD, provides the clock that clocks the third byte into the input/output data buffer, and clocks the counter of the loop test SYNC counter function. The loop test SYNC function generates a *loop test SYNC* signal (TLPT1A) that clocks the third byte loop test signal out of the input/output data buffer.

(1) *Output from register command (OFR CMD) decoder and latch*. When the OFR CMD signals (TXS3BP, TXS4BQ, TXS5BP, TXS6BP, and TXS7BP) and the *hardware busy=L* signal (TBUSYR) are high and the *CMD PH 2nd byte* signal (TXCA10O) goes high, the OFR CMD is latched. When the *1st and 2nd byte= H* signal (TXXB1P) is high, and the latch is set, the *OFR set** output signal (TXODRA) is produced. When the latch is set during the third byte, the *third byte=H* signal (TXXB1Q) is present. When the *state count 5* (TXXAOP) and *state count 2* (TXXA1Q) signals go high, the *input register clock* (REG CLK) signal (TXOD0A) goes low. When the *2nd and 3rd byte = H* signal (TXXB0Q) goes low at the end of the third byte, the latch is reset. With the latch' reset, TXOD0A and TXODRA are forced to remain high until a new OFR CMD occurs.

(2) *Loop test sync counter*. The -counter consists of two flip-flops that are reset by the *master reset* signal (TXRS2B). When the *input register clock (REG CLK)* (TXOD0A) goes low, the first flip-flop is set, providing a high input to the second flip-flop and forcing the *loop test = L* output signal (TLPT0P) low. The next *1-MHz PH1* clock (TXCQ1B) clocks the high through to the output of the flip-flop. With the output of the second flip-flop set to high, the next high *1-MHz PH2* clock (TXCQ3B) gates out the low *loop test synchronizer (SYNC)* signal (TLPT1A). Signal TXCQ1B occurs 0.5 **µ**s prior to TXCQ3B. When the TXCQ3B clock goes low, TLPT1A goes high. Signal TLPT1A is also the clock for the first flip-flop. When it goes high, the *MTS disable=H/ normal = L* signal (TXGN1A) is clocked through the first flip-flop to the second flip-flop. The low logic level is clocked through the second flip-flop by the next TXCQ1B forcing TLPT1A high. This, in effect, resets the counter until another OFR CMD occurs.

c. End of Block Command (EOB CMD) Decoder with Synchronizer (SYNC) Counter. For read or write functions of the MTU, the ADP sends the EOB command. The execution of the first two bytes of the EOB command phase are explained in this paragraph. During the third byte of the command, the length of the blocks of read or write data are set in the EOB counter. For an explanation of the function during the third byte, refer to the description of the end of block counter (para. 5-24). Initially, the master reset signal resets the SYNC counter. If the *EOB command* signals (TXS3BP, TXS4BP, TXS5BP, TXS6BQ, and TXS7BP) are high when the *CMD PH 2nd byte* signal (TXCA10) goes high, the output of the first flip-flop of the SYNC counter is set high. This high logic level is clocked through to the output of the second flip-flop of the counter by the *1-MHz PH1* clock (TXCQ1B) to produce the *SYNCED EOB CMD* output signal (TXEB1Q). With TXEB1Q high, the trailing edge of the next *1-MHz PH2* clock (TXCQ3B) clocks the low TXGN1A signal through the first flip-flop to the input of the second flip-flop. Signal TXCQ1B occurs 0.5 µs prior to TXCQ3B. The next TXCQ1B clocks the low through the second flip-flop, forcing TXEB1Q low. This, in effect, resets the SYNC counter.

d. Stop Command (CMD) Decoder with Synchronizer (SYNC) Counter. The *stop/space record (SPA REC)=H* signal (TSPAO1) goes high when TXS5BP, TXS6BP, and TXS7BQ are high. These signals, along with TXS3BP and TXS4BP, make up the stop command signals. If the stop command signals are high when TXCA10 goes high, the output of the level is clocked through the second flip-flop of the counter by the next TXCQ1B clock. This high flip-flop output allows the high TXCQ3B to clock out the low *synchronized stop command (SYNCED stop CMD)* signal (TXST1A). Signal TXST1A goes to the state and byte counter logic

where it becomes one of the inputs that generates the master reset signals. When TXCQ3B goes low, TXST1A goes high and clocks the low TXGN1A through the first flip-flop to the second flip-flop. The low logic level is clocked through the second flip-flop by the next TXCQ1B. This forces TXST1A high and resets the counter.

e. Input From Register Command (IFR CMD) Decoder Gate. The IFR CMD is used by the ADP to command that the status of the MTU be sent to the ADP. When the *IFR CMD* signals (TXS3BP, TXS4BP, TXS5BQ, TXS6BP, and TXS7BP) are high, and TXCA1O goes high during the second byte, the *IFR CMD* output signal (TXIR0A) goes low. Signal TXIR00A goes to the read, status, or interrupt output logic where it enables the status data byte. The status data byte is sent to the I/O interface and then to the ADP.

5-17. Start/Stop Control Logic (fig. 5-20). The start/stop control logic is located in the card cage. The purpose of this logic is to provide start and stop delays in the execution times of the device commands. This allows the MTT the necessary time to run up to proper speed for transferring data. It also allows the MTT the necessary time to slow to a stop. This logic also prevents unnecessary stops if a new command is received within 5 ms of the end of the previous command. At the proper times, this logic provides some of the conditional signals for actuating the read and write functions. This logic consists of the following eight major circuit functions.

End-of-command interrupts and hardware/ software busy
Look ahead counter
Device command syncronizer (SYNC) counter
Start delay counter
Stop delay counter
Flying start delay
Old/new speed/direction comparator
Run/stop latch and tape direction indicators

a. End-of-Command Interrupts and Hardware/ Software Busy (fig. 5-20). Software busy indicates that the ADP is processing the next input to the MTU. Hardware busy indicates that the MTT is in a ready to run state. The interrupts are control signals determined by the end of a command or the MTT detecting the end or beginning of the tape. These signals are provided by the software busy detect OR gate, hardware busy detect circuit, and interrupt detect circuit.

(1) *Interrupt detect*. The *end read/write* (TNSGAA), *end space command (CMD*) (TSPC1A), *high speed end of block command* (HI-SP EOB CMD) (THSC1A), *end erase forward command (end ERS FWD CMD)* (TERC1A), set no data error flip-flop (FF) (TNDTSA), or *new command (CMD) rejected* (TSCI1A) signals activate the low *end of command interrupt (INT)* output signal (TINT1A). When the *low speed (SP)=H* signal (THISPP) is active with one of the end of command inputs, the end of *low speed command interrupt (SP CMD INT*) output signal (TINT2A) occurs simultaneously with TINT1A. When the *forward direction (FWD DIR) = H* signal (TDIRIS) is active and the tape reaches the end of tape, the *end of tape counter (EOT CTR) bit 1* signal (TEOT1S) goes high and enables the output; then, when the *1-MHz PH2* clock (TXCP3B) goes high, the *forward end tape interrupt (FWD EOT INT)* output signal (TINT7A) is produced. Either TINT7A or the combination of high signals *beginning of tape counter (BOT CTR) bit 1* (TBOT1S), *reverse direction (REV DIR)=H* (TDIRIR), and TXCP3B produces the *forward end of tape/reverse beginning of tape (FWD EOT/REV BOT) detect interrupt (INT)* output signal (TINT5A). When the *low speed (SP)=H* signal (THISPP) is active, the logic for TINT5A also produces the *low speed forward end of tape (FWD EOT)* detect interrupt (INT) output signal (TINT6A). Each of the outputs is an active low 250-ns strobe.

(2) *Software busy detect OR gate*. If the *end of low speed command interrupt (SP CMD INT) (TINT2A), low speed forward end of tape (FWD EOT) detect interrupt (INT) (TINT6A), loop test=L* (TLPT0P), *interrupt wait for enable** (TXXDIR), *loop test or read wait for enable** (TXXDDR), or *low = new command received* (CMD RCVD) (TSNCOR) signals go low, the *software busy* signal (TSBZYO) goes high, indicating that the MTU is waiting for an input from the ADP.

(3) *Hardware busy detect*. The low *MTT ready to receive (RCV)** signal (XRDY1A) is inverted to produce the high *MTT ready to RCV* output signal (TRDY1O). There are four combinations of the *forward (FWD)=H* (TDIRSQ), *reverse (REV)=H* (TDIRSP), *end of tape=H* (TEOT0S), and *begin of tape=H* (TBOT0S) signals which, along with the high *if file protect error (FPE), erase/write inhibit = L* (TFPE2A), *volts to read/write heads* (TSNC1S),

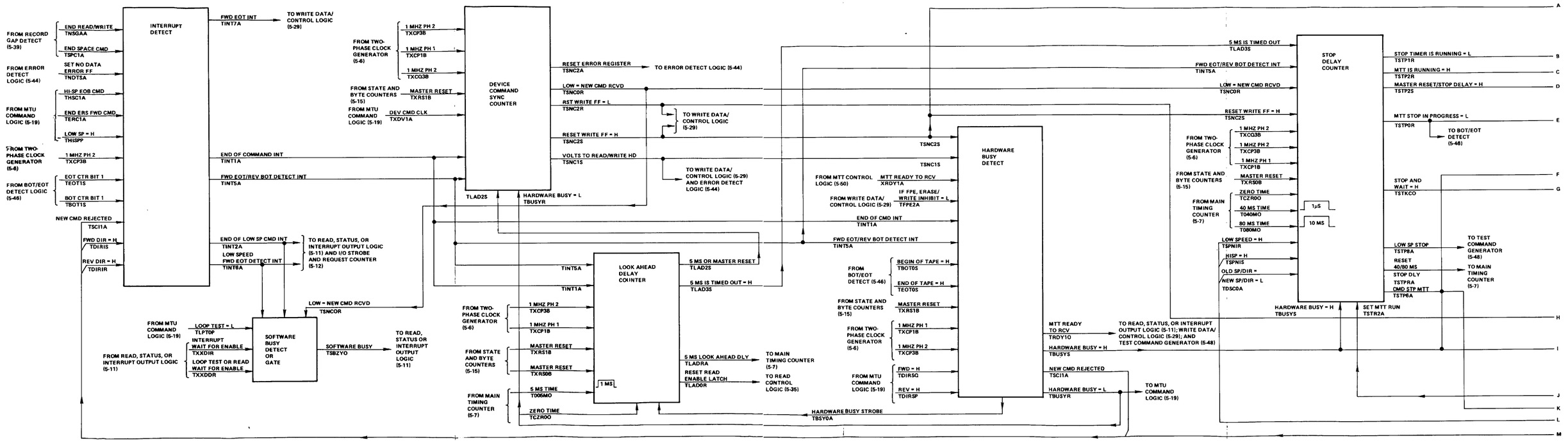

Figure 5-20. Start/Stop Control Block Diagram (Sheet 1 of 2)

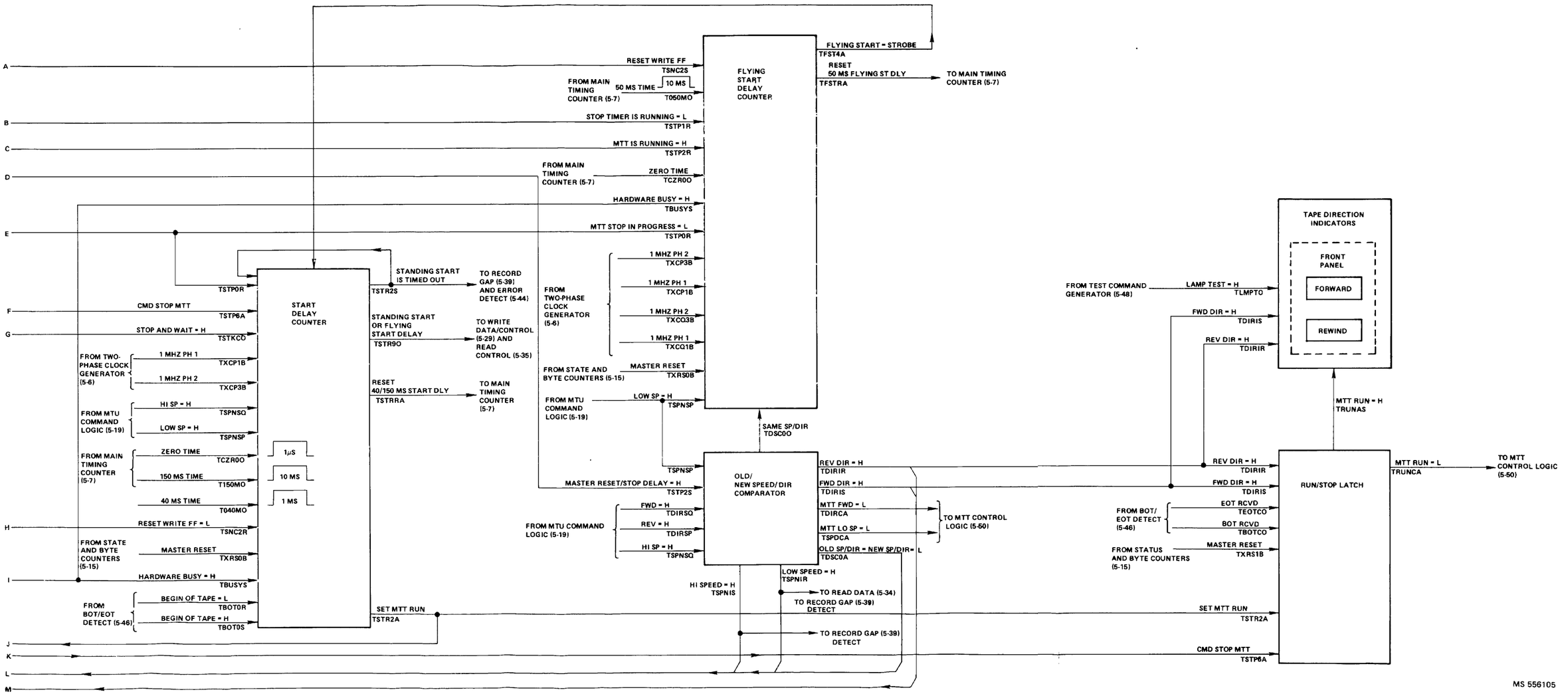

Figure 5-20. Start/Stop Control Block Diagram (Sheet 2 of 2)

TRDY1O, and *1-MHz PH1* clock signal (TXCP1B), provide the active low *hardware busy strobe* (TBSY0A). Signal TBSY0A sets the *hardware busy = H* output signal (TBUSYS) and the *hardware busy = L* output signal (TBUSYR). Signal TBUSYR is reset high prior to being set by the end of command interrupt (CMD INT) (TINT1A), forward end of tape/reverse beginning of tape (FWD EOTIREV BOT) detect interrupt (INT) (TINT5A), or *master reset* (TXRS1B) signals. If TBSY0A does not set TBUSYR low when the *reset write flip-flop (FF) = H* signal is activated, the next high *1-MHz PH2* clock (TXCP3B) produces the *new command (CMD) rejected* output signal (TSCI1A). The four combinations of TDIRSQ, TDIRSP, TEOT0S, and TBOT0S to produce TBSY0A are as follows:

TDIRSQ (high) and TBOT0S (high)
TDIRSP (high) and TEOT0S (high)
TDIRSQ (high), TBOT0S (low), and TEOT0S (low)
TDIRSP (high), TBOT0S (low), and TEOT0S (low)

b. Look Ahead Delay Counter (fig. 5-20 and 5-21). The *master reset* signal (TXRS0B) sets the *5-ms or master reset* signal (TLAD2S) to high and resets the *5-ms is timed out = H* signal (TLAD3S) to low. When the *hardware busy=L* signal (TBSY0A) goes low, TLAD2S is reset low. The *master reset* signal (TXRS1B) resets the *reset read enable latch* output signal (TLAD0R) to high and TLAD0S to low. The *low* TLAD0S *resets* TLAD1R to high. Either the low *end of command interrupt (CMD INT)* signal (TINT1A) or the low *forward end of tape/reverse beginning of tape (FWD EOT/REV BOT) detect interrupt (INT)* signal (TINT5A) sets TLAD0S to high. The high TLAD0S and the high TLAD1R produce the 50-ns 5 *ms look ahead delay* output strobe (TLADRA). The low TLADRA resets the main timing counter to zero, which produces the high *zero time* signal (TCZR0O). With TCZR0O and TLAD0S high, the active high *1-MHz PH1I* clock (TXCP1B) produces the low strobe TLAD0A. Signal TLAD0A sets TLAD1S to high and TLADIR to low. The main timing counter, after 5 ms from time zero, provides the high *5-ms time* signal (TO05MO). The next TXCP1B produces the low TLAD2A strobe. Signal TLAD2A sets TLAD2S and TLAD3S to high. The high TLAD2S and the next *1-MHz PH2* clock (TXCP3B) produces the low strobe TLAD1A. Signal TLAD1A resets TLAD0S to low and TLAD0R to high. The low TLAD0S resets TLADIR to high, which enables the TLADRA output in preparation for the interrupts TINT1A and TINT5A. These interrupts occur at the end of the present command. The interrupts start the counter sequence again, providing the 5-ms time during which a new command must be received by the MTU, or the MTT will stop.

c. Device Command Synchronizer (SYNC) Counter (fig. 5-20 and 5-22). Initially, the *master reset* signal (TXRS1B) resets the *low=new command received (RCVD)* signal (TSNC0R) to high and its internal complement signal (TSNC0S) to low. After one or more commands, either the *end of command interrupt (CMD INT)* signal (TINT1A) or the *forward end of tape/reverse beginning of tape (FWD EOT/REV BOT) detect interrupt (INT)* signal (TINT5A) actuates the reset. When the *device command clock (DEVCMD CLK)** signal (TXDV1A) goes low, the leading edge of the 62.5-ns pulse sets TSNC0S to high and TSNCOR to low. Initially, the *5-ms or master reset* signal (TLAD2S) goes high with the master reset. For commands after the initial command, TLAD2S goes high 5 ms after TSNCOR is reset high. If TXDV1A sets TSNCOR low during this 5 ms, the low TSNCOR output to the stop delay counter prevents the stop sequence from continuing. The *reset write flip-flop (FF)=L* signal (TSNC2R) is reset high at the completion of the counter cycle. The *hardware busy=L* signal (TBUSYR) is high prior to setting up the MTT for running. Initially, with TLAD2S, TSNC2R, and TBUSYR high, when TSNC0S goes high, the next *1-MHz PH2* clock (TXCQ3B) produces an internal active low strobe signal TSNC0A. For commands that follow the initial command with TSNC2R, TBUSYR, and TSNC0S high, when TLAD2S goes high, the next TXCQ3B clocks out TSNC0A. Signal TSNC0A sets the *volts to read/write head (HD)* signal (TSNC1S) to high and its internal complement signal to low. With TSNC1S high, TBUSYR from the hardware busy block goes low on the next TXCP1B clock signal. The active low strobe *reset error register* (TSNC2A) is also produced. Signal TSNC2A sets the *reset write flip-flop (FF) = H* signal (TSNC2S) to high and the *reset write flip-flop (FF)=L* signal (TSNC2R) to low. When TSNC2S goes high, the next *1-MHz PH2* clock (TXCP3B) produces the low internal signal TSNC1A. Signal TSNC1A resets two other internal signals; TSNC1R to high and TSNC1S to low. With TSNC1R high, the next TXCP1B clock produces the low internal signal TSNC3A. Signal TSNC3A resets TSNC2R high and TSNC2S low.

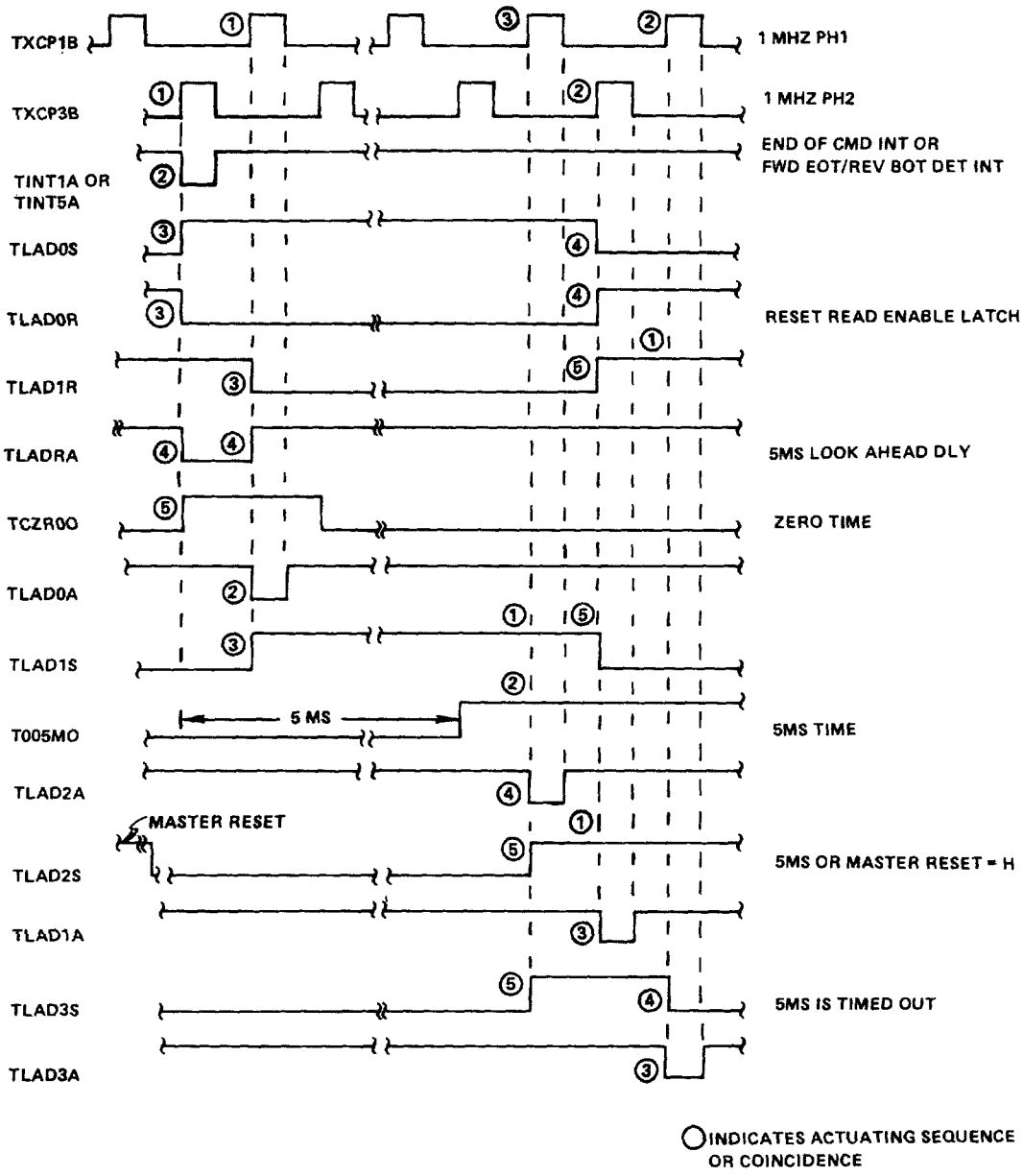

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Figure 5-21. Look Ahead Delay Counter Timing Diagram

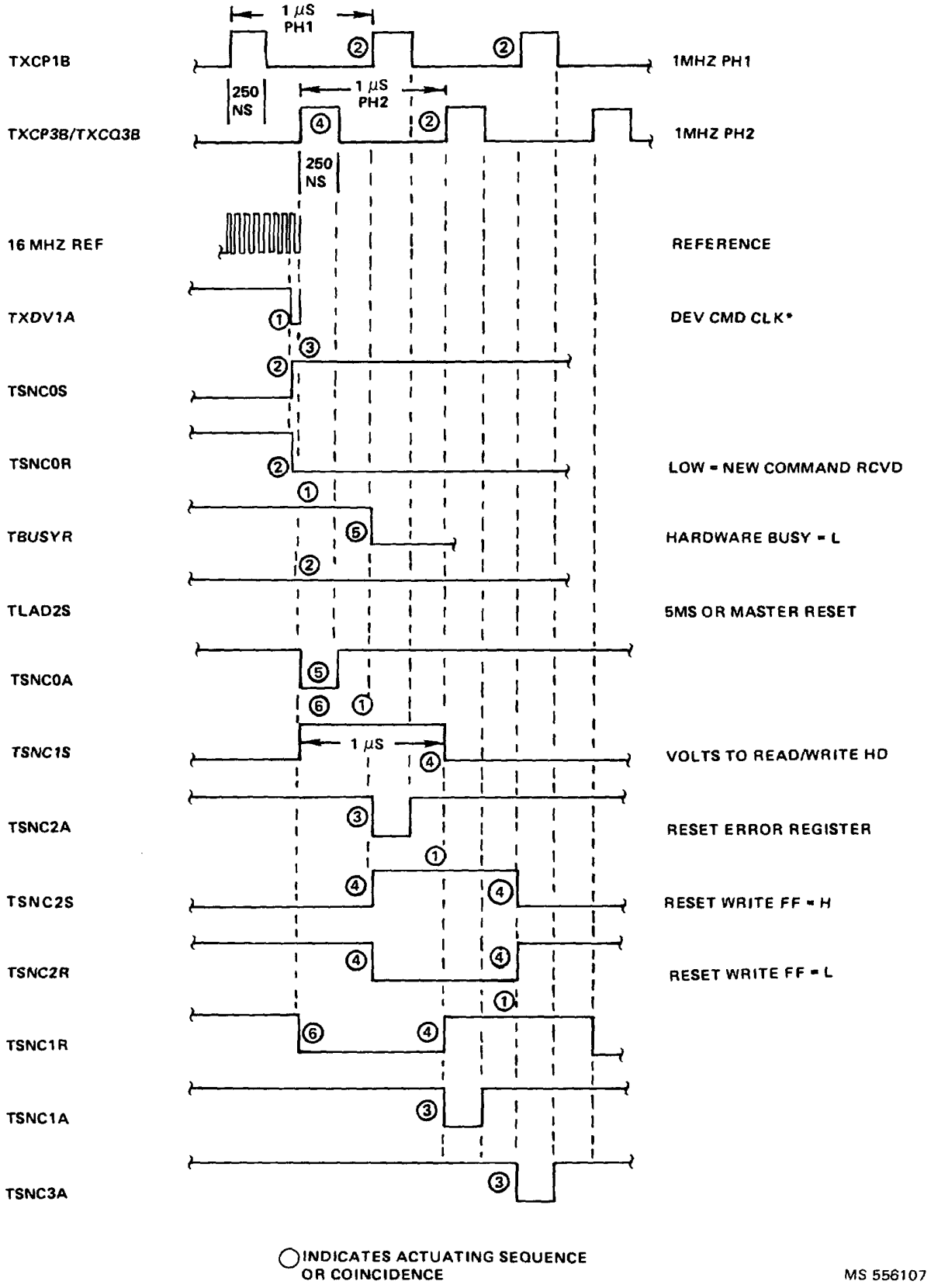

Figure 5-22. DEV CMD SYNC Counter Timing Diagram

d. Start Delay Counter (fig. 5-20 and 5-23). The start delay counter provides time delays in the execution of commands. The delays allow a break in the execution while the MTT runs up to speed. There is a 150-ms delay for standing start from the beginning of the tape (BOT), a 40-ms delay for runup to high speed from a standing start when not at BOT, a 40-ms delay for runup to low speed from a standing start when not at BOT, and a flying start delay provided by the flying start delay counter. The function of the counter is described in four parts; reset, set, time delays, and timed out.

(1) *Counter reset (fig. 5-20 and 5-23).* The counter is reset two ways. In the first way, when the *hardware busy=H* signal (TBUSYS) is low (caused by a master reset or end of command), the internal signal TSTR0S is reset low. In the second way, when the counter times out, the *standing start is timed out* signal (TSTR2S) goes high; on the next *1-MHz PH2* (TXCP3B) clock pulse, TSTR0S is reset low. The low TSTR0S resets internal signal TSTR1R to high. Signal TSTR1R is also reset to high when the *MTT stop in progress=L* signal (TSTP0R) goes low. The *master reset* (TXRS0B) or *CMD stop MTT* (TSTP6A) signals reset the counter *standing start is timed out* output signal (TSTR2S) to low.

(2) *Counter set (fig. 5-20 and 5-23).* With the stop and wait=H (TSTKC0), *reset write flip-flop (FF)=L* (TSNC2R), and *hardware busy=H* (TBUSYS) input signals all high, the next *1-MHz PH2* clock (TXCP3B) produces internal signal TSTR0A which resets another internal signal TSTR0S to high. With the *MTT stop in progress=L* (TSTP0R) and TSTR1R signals both high when TSTR0S goes high, the *reset 40/150-ms start delay* output signal (TSTRRA) goes low. The low TSTRRA goes to the main timer where it resets the timer to zero. The main timer then sends the high *zero time* signal (TCZR0O) to the start delay counter. With TSTR0S, TSTP0R, and TCZR0O high, the next *1-MHz PH1* clock (TXCP1B) produces the active low output strobe *set MTT run* (TSTR2A). Signal TSTR2A sets TSTR1R to low (which produces the trailing edge of the TSTRRA signal) and sets TSTR1S to high.

(3) *Time delays*. There are time delays for standing start at beginning of tape (BOT) and standing start not at BOT.

(a) Standing start at BOT (fig. 5-20 and 523). If the *beginning of tape = H* signal (TBOT0S) is high when internal signal TSTR1S goes high, the internal strobe TSTR3A goes low. The low TSTR3A sets TSTR3S to high. When the MTT runs, the tape moves away from the beginning of the tape and the *begin of tape=L* signal (TBOT0R) goes high. When the elapsed time from time zero reaches 150 ms, the *150-ms time* signal (T150MO) goes high. With TSTR3S, TBOT0R, and T150MO high, the next *1-MHz PH1* clock (TXCP1B) produces the internal active low strobe TSTR4A.

(b) Standing start not at BOT (fig. 5-20 and 5-23). There is a separate but equal time delay for high speed and low speed.

1 *Low speed delay*. The high TSTR1S enables the delay gate and resets TSTR3R to high. A low speed command activates the *low speed (SP)=H* signal (TSPNSP) to high. With TSTR1S, TSTR3R, and TSPNSP high, when the *40-ms time* signal (T040MO) goes high, the next TXCP1B clock pulse produces the active low internal strobe signal TSTR6A.

2 *High speed delay*. The high TSTR1S resets TSTR3R to high. A high command activates the *high speed (HI SP) =H* signal (TSPNSQ) to high. With TSTR1S, TSTR3R, and TSPNSP high when the *40-ms time* signal (T040MO) goes high, the next TXCP1B clock pulse produces the active low internal strobe TSTR8A.

(4) *Timed out counter*. Any of the time delay outputs (TSTR4A, TSTR6A, or TSTRBA) or the *flying start* strobe (TFST4A) produces the *standing start* or *flying start delay* output signal (TSTR90). Signals TSTR4A, TSTR6A, or TSTR8A also set the standing *start is timed out* output signal (TSTR2S) to high.

e. Stop Delay Counter (fig. 5-20, 5-24, and 5-25). The stop delay counter provides two delays (high speed and low speed) during which the MTT slows to a stop. The stop is initiated either by a command that changes direction or speed of the MTT by an end-of-command (when no new command is received within 5 ms) or by the interrupt generated at the end of tape (EOT) in the forward direction or the beginning of tape (BOT) in the reverse direction. The function is subdivided into five subfunctions as follows:

Counter reset
Counter set
Timer start
Time delays
Timed out

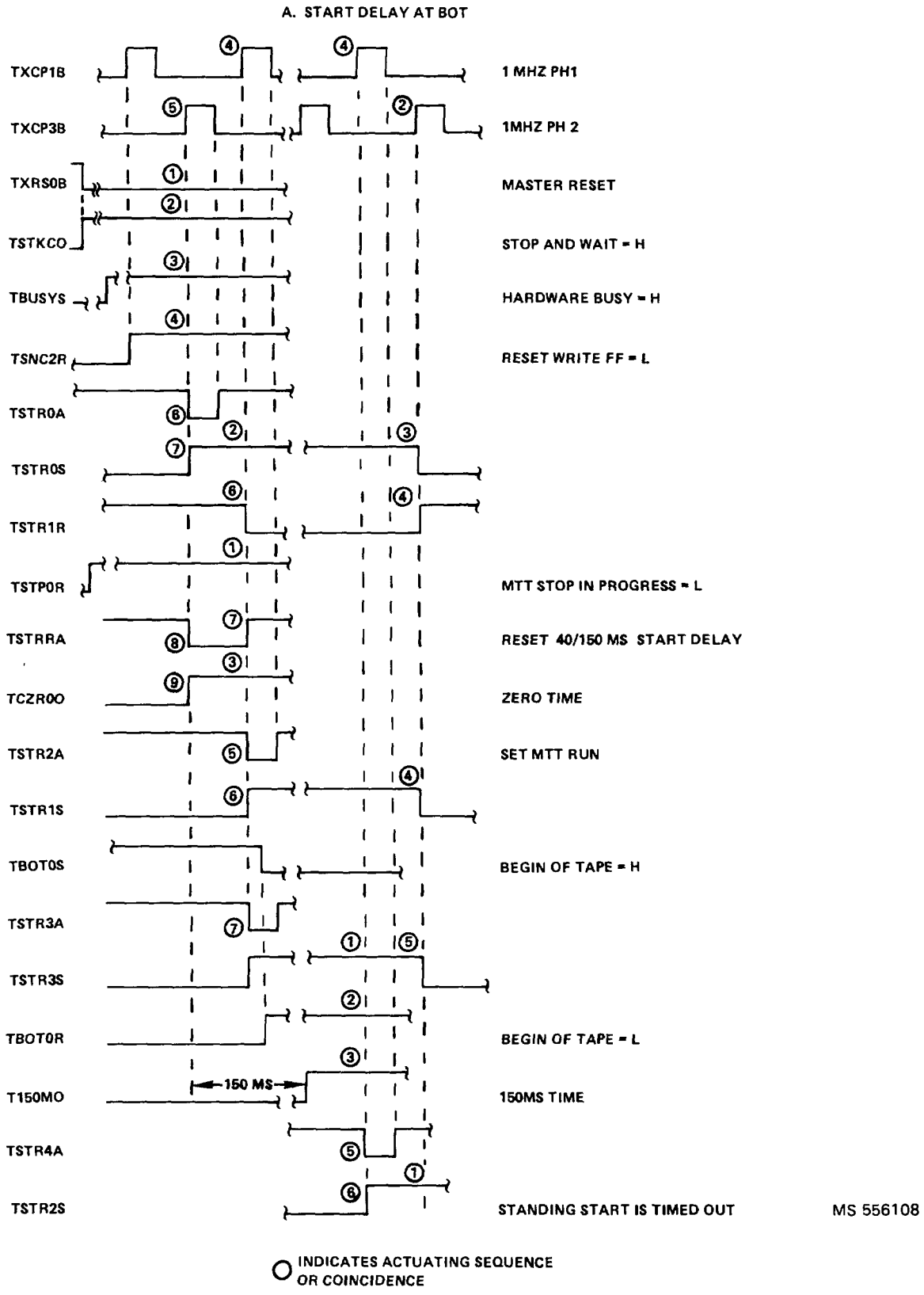

Figure 5-23. Start Delay Counter Timing Diagram (Sheet 1 of 2)

b. LOW SPEED START NOT AT BOT

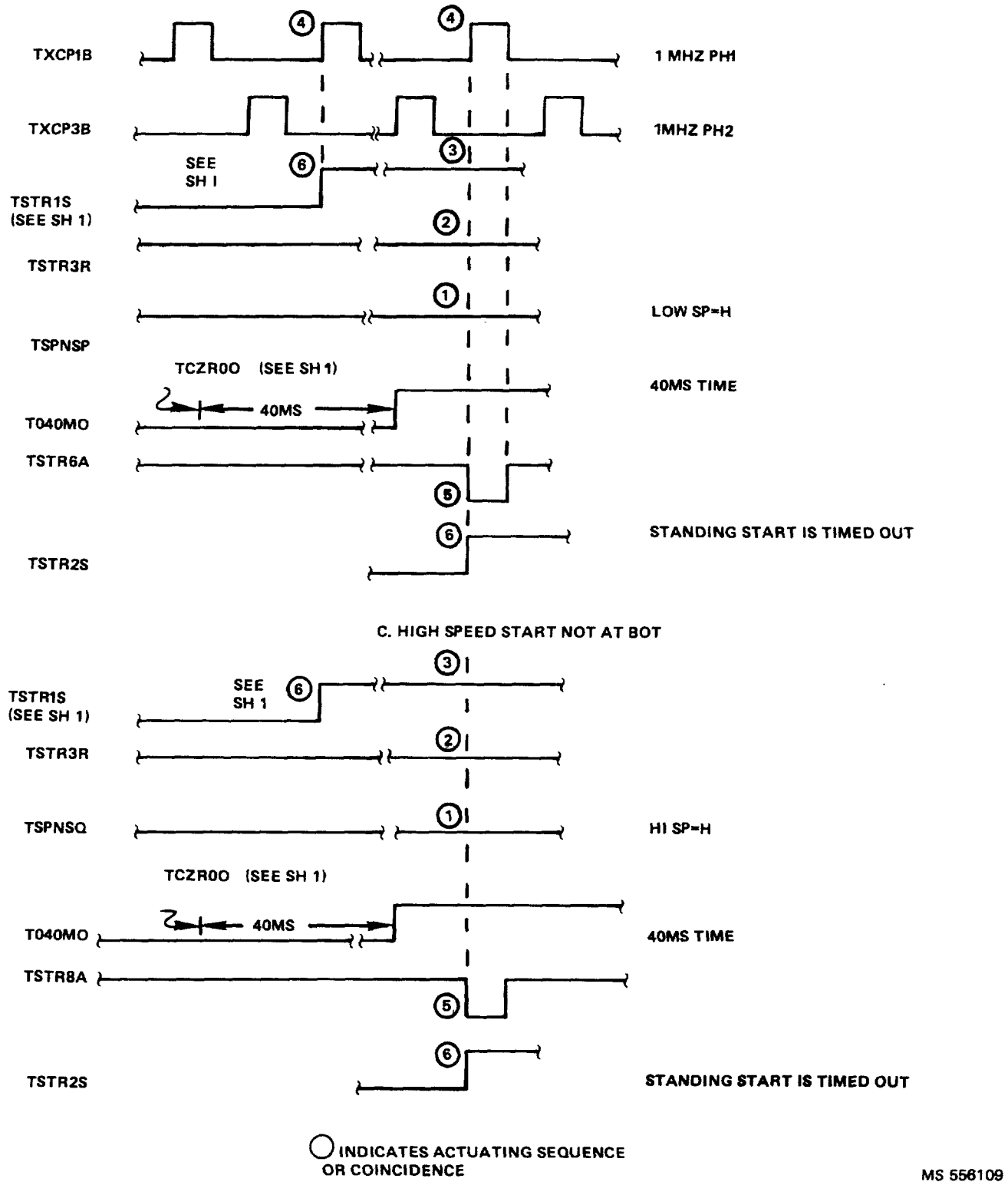

Figure 5-23. Start Delay Counter Timing Diagram (Sheet 2 of 2)

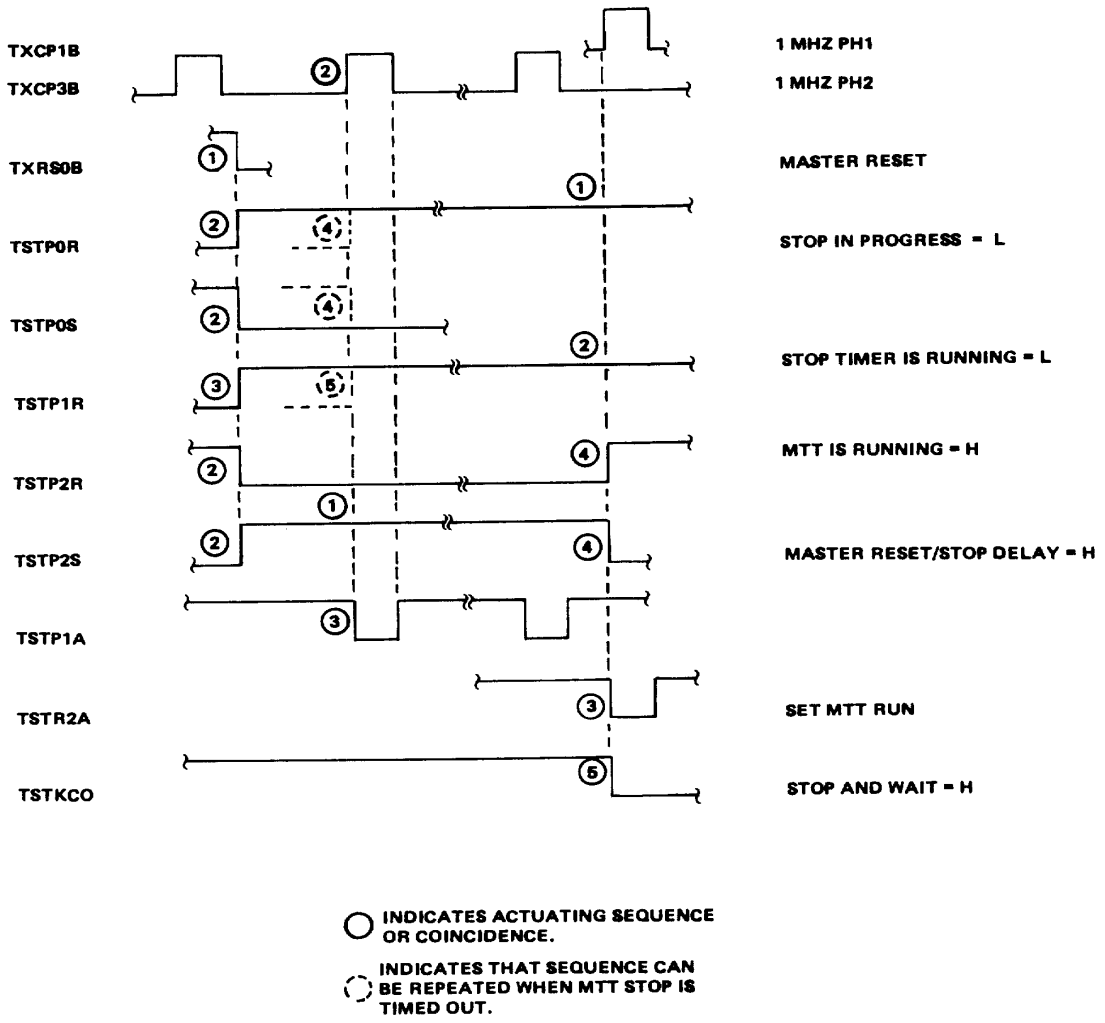

Figure 5-24. Stop Delay Counter Reset Timing Diagram

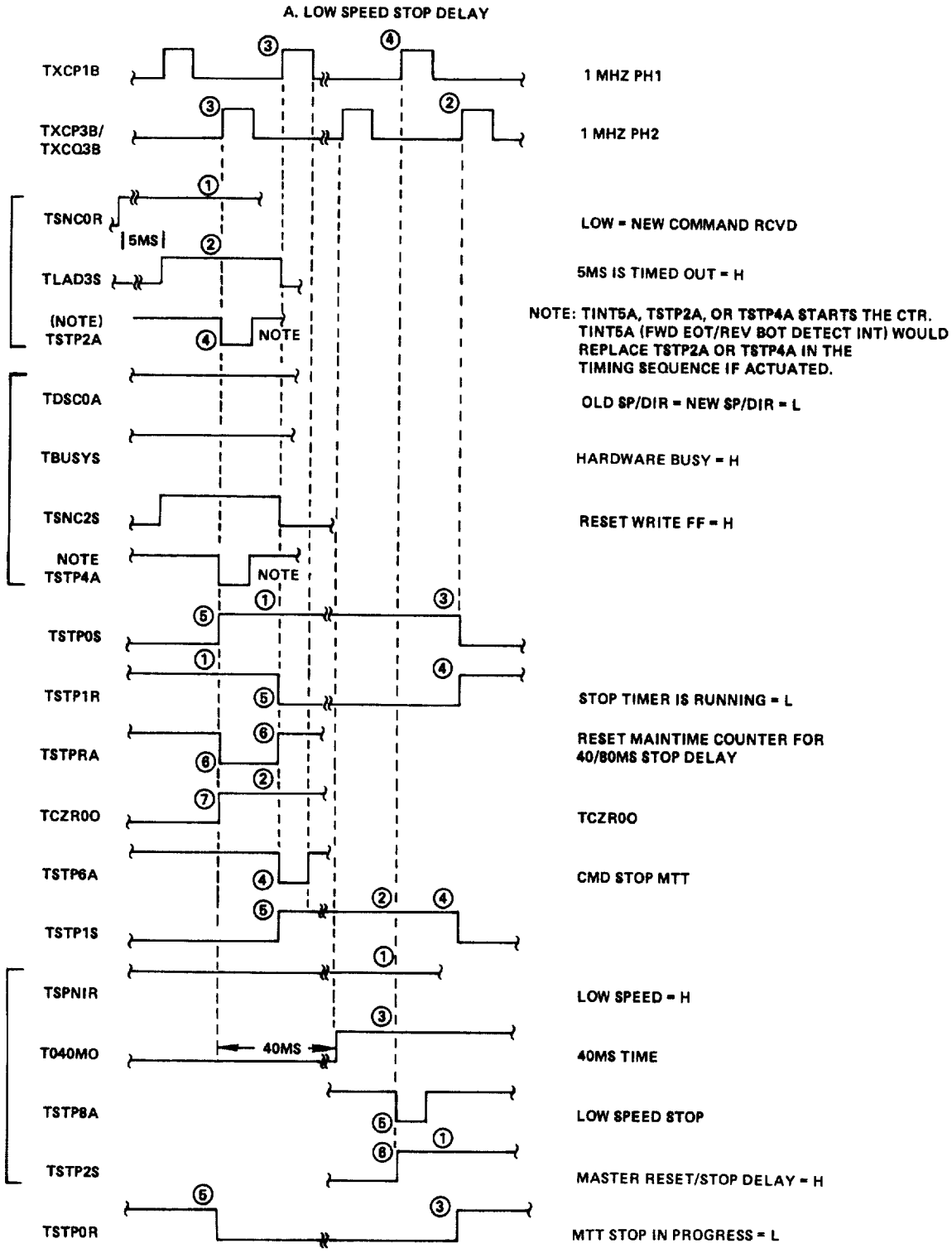

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Figure 5-25. Stop Delay Counter Timing Diagram (Sheet 1 of 2)

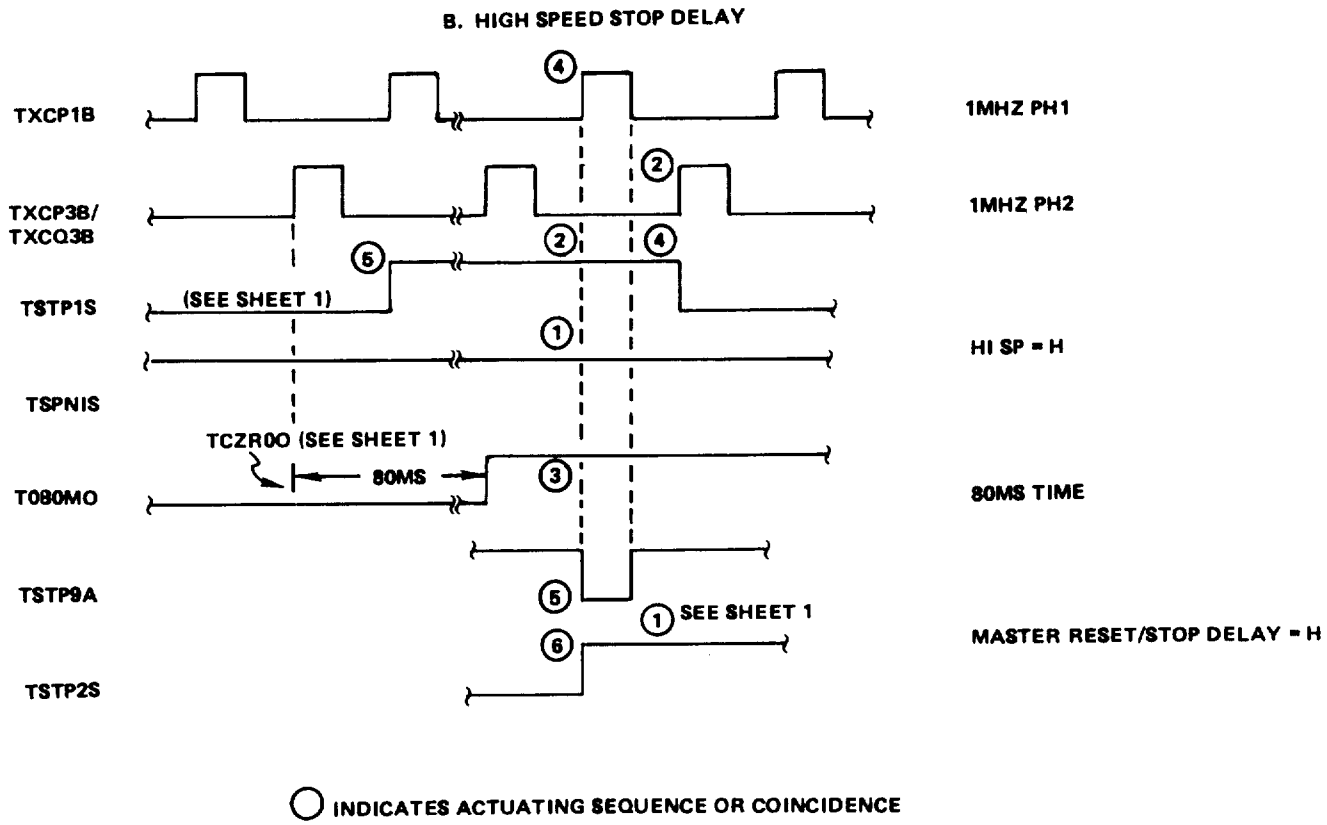

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Figure 5-25. Stop Delay Counter Timing Diagram (Sheet 2 of 2)

(1) *Counter reset (fig. 5-20 and 5-24).* The *master* reset signal (TXRS0B) resets the *MTT stop in progress = L* signal (TSTP0R) to high and its internal complement signal TSTP0S to low. Also, TSRSOB sets the MTT is *running = H* signal (TSTP2R) to low and *master reset/stop delay = H* signal (TSTP2S) to high. With TSTP2S high, the next *1-MHz PH2* (TXCP3B) clock pulse produces the active low internal strobe signal TSTP1A. Signal TSTP1A (after the counter completes a cycle) also resets TSTP0R to high and its internal complement signal TSTP0S to low. The low TSTPOS resets *stop timer* is running =L (TSTP1R) to high. The *set MTT run* signal (TSTR2A) from the start delay counter goes to the MTT; it also resets TSTP2S to low and TSTP2R to high. With TSTPOR, TSTP1R, and TSTP2R all high, the *stop and wait* = H output signal (TSTKCO) goes low. The low TSTKCO indicates that the stop delay counter is ready for the stop sequence to be initiated.

(2) *Counter set (fig. 5-20 and 5-25).* Signal TSTP0S is set high by the active low interrupt *forward end of tape/reverse beginning of tape* (FWD EOT/REV BOT) *detect interrupt* (INT) signal (TINT5A) or the active low internal strobe signals TSTP2A or TSTP4A. If the *low = new command* received (RCVD) signal (TSNC0R) remains high until the *5 ms is timed out = H* signal (TLAD3S) goes high, the next 1 -MHz PH2 clock (TXCP3B) produces TSTP2A. If the old speed/direction (SP/DIR)=new SPIDIR=L signal (TDSC0A) is high (indicating a speed or direction change) and the *hardware busy = H* signal (TBUSYS) is high when the reset write flip-flop (FF)=H signal (TSNC2S) goes high, the next *1-MHz PH2* clock (TXCQ3B) produces TSTP4A. Signal TINT5A is provided by the interrupt detect block.

(3) *Timer start (fig. 5-20 and 5-25).* With TSTP1R high, when TSTP0S is set high by TSTP2A, TSTP4A, or TINT5A, the reset maintime counter for the *40/80-ms stop delay* output signal (TSTPRA) goes low, producing the high *zero time* input signal (TCZR0O) from the main timing counter. With TSTP0S and TCZR0O high, the next *1-MHz PH1* clock (TXCP1B) produces the active low CMD stop MTT output strobe (TSTP6A). Signal TSTP6A sets TSTPIS to high.

(4) *Time delays (fig. 5-20 and 5-25).* The counter produces two time delays; 40 ms for low speed and 80 ms for high speed.

(a) *Low speed delay (fig. 5-20 and 5-25). With* TSTP1S and the *low speed = H* signal (TSPNIR) both high, when the elapsed time from TCZR0O is *40 ms*, the high 40-ms time signal (T040MO) is produced, and the next *1-MHz PH1* clock (TXCP1B) produces the active low *low speed stop* output strobe (TSTP8A).

(b) *High speed delay (fig. 5-20 and 5-25).* With TSTP1S and the *high speed (HI SP)=H* signal (TSPNIS) both high, when the elapsed time from TCZR0O is 80 ms, the high *80-ms* time signal (T080MO) is produced, and the next TXCP1B clock pulse produces the active low internal strobe signal TSTP9A.

(5) *Timed out (fig. 5-20, 5-24, and 5-25).* Any one of the TSTP8A, TSTP9A, or *master reset* (TXRS0B) signals sets the *master reset/stop delay = H* output signal (TSTP2S) to high. For a continuation of the description of this function when set it is by TXRSOB, refer to paragraph 517e(1).

f. Flying start delay counter (fig. 5-20 and 5-26). When a new command is received within 5 ms of the end of the previous command and the new command requires the same low speed and direction, the 50-ms start delay is initiated. The function is divided into two subfunctions; reset and set.

(1) *Counter reset.* Initially, the *master reset* signal (TXRS0B) resets to low the internal output signal TFST2S of the last stage of the counter. At the completion of a cycle of the flying start delay counter, TFST2S is set high. The next *1-MHz PH2* clock (TXCQ3B) produces the active low internal signal TFST1A. Either the low TFST1A or (initially, when the MTT is not ready) the *low hardware busy = H* signal (TBUSYS) resets internal signal TFST0S to low. The low TFST0S resets internal signal TFST1R to high. With TFST1R high, the next *1-MHz PH1* clock (TXCQIB) produces the active low internal strobe signal TFST3A. Signal TFST3A resets TFST2S to low.

(2) *Counter* set. When the low speed *(SP)= H* (TSPNSP), *same speed/direction (SP/DIR)* (TDSC0O), *hardware busy = H* (TBUSYS), *MTT stop in progress = L* (TSTP0R), *stop timer is running = L* (TSTP1R), *MTT is running =H* (TSTP2R), and *reset write flip-flop (FF)* (TSNC2S) signals are all high, the next 1-MHz PH2 clock (TXCP3B) produces the active low internal strobe signal TFST0A. Signal TFST0A sets TFST0S to high. With TFST1R high, when TFST0S goes high, the *reset 50-ms flying start delay* output signal (TFSTRA) goes low. The low TFSTRA to the main timer results in the high *zero time* signal (TCZR0O).

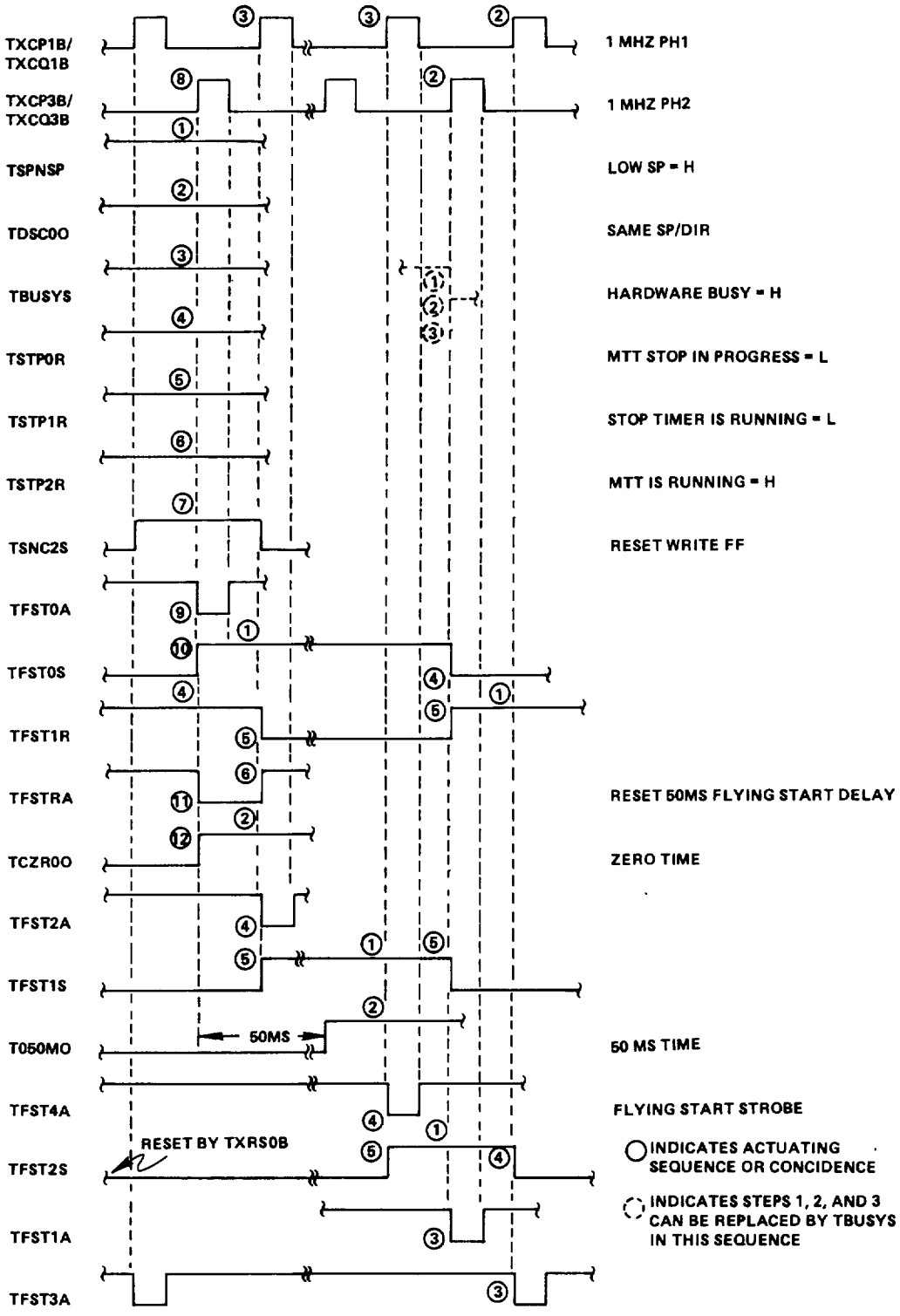

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Figure 5-26. Flying Start Delay Counter Timing Diagram

With TFST0S and TCZR0O high, the next *1-MHz PH1* clock (TXCP1B) produces the active low strobe TFST2A. Signal TFST2A sets TFST1R to low and thereby produces the trailing edge of the signal TFSTRA and sets TFST1S to high. With TFST1S high, when the elapsed time from internal signal TCZR0O equals 50 ms, the 50ms time signal goes high. The next *1-MHz PH1* clock (TXCP1B) produces the active low output *flying start strobe* (TFST4A). Signal TFST4A also sets TFST2S to high. Refer to paragraph 5-17f(1) for a description of the use of TFST2S as a reset subfunction.

g. *Old/New/Speed/Direction (DIR) Comparator (fig. 5-20).* The function of this logic is to stop the tape if the new command causes either the speed or direction of the tape to change or allow the tape to continue running if the new command calls for the same speed and direction. Initially, the *master reset/ stop delay* = H signal (TSTP2S) goes high on master reset. The command follows immediately, which provides the forward (FWD) = H (TDIRSQ), *reverse* (REV) = H (TDIRSP), *high speed (HI SP)=H* (TSPNSQ), or *low speed (SP) = H* (TSPNSP) signals. The high TSTP2S is coincident with one of those four signals producing one of the corresponding signals forward direction (FWD DIR) = H (TDIRIS), reverse direction (REV DIR) = *H* (TDIRIR), *HI speed = H* (TSPNIS), or *low speed = H* (TSPNIR). There are four combinations of high inputs that can produce the *same speed/direction (SPIDIR)* signal (TDSC0O). Initially, one of the four are set. The first combination of high signals includes TDIRSQ, TDIRIS, TSPNSQ, and TSPNIS. The second combination of high signals includes TDIRSQ, TDIRIS, TNSPNP, and TSPNIR. The third combination consists of high signals TSPNSQ, TDIRSP, TDIRIR, and TSPNIS. The fourth combination of high signals that produces the high TDSCOO includes TDIRSP, TDIRIR, TSPNIR, and TNSPNP. Signal TDSCOO is inverted to produce the low *old SP/DIR = new SPIDIR = L* output signal (TDSCOA). Subsequent commands while the tape is running find the signal TSTP2S at a low level. Therefore, the logic levels of the new input commands TDIRSQ, TDIRSP, TSPNSQ, or TSPNSP change if speed or direction change. The same signals do not change if speed and direction remain the same; also, the latched output signals TDIRIS, TDIRIR, TSPNIS, and TSPNIR remain at the same level. Consequently, if speed and direction change, none of the four combinations previously mentioned provide the logic levels for the high TDSC0O. The low TDSC0O and the high TDSC0A indicate a new speed or direction which results in the tape stopping even though a new command is received within 5 ms. When the stop delay has timed out, TSTP2S goes high and sets or resets the latched signals TDIRIS, TDIRIR, TSPNIS, or TSPNIR to the new level corresponding to the new command. If the new command is the same as the old command, the command signals TDIRSQ, TDIRSP, TSPNSQ, and TSPNSP remain the same and the output signal TDSC0O remains high. Also, TDSC0A remains high indicating that the new speed/direction equals the old speed/direction and the tape continues running.

h. Run/Stop Latch and Tape Direction Indicators (fig. 5-20). The run/stop latch generates the run control signal for the MTT, and the indicators on the front panel indicate the direction of tape movement.

(1*) Run/stop latch.* The *set MTT run* signal (TSTR2A) sets the *MTT run =H* signal (TRUNAS), which enables the tape direction indicators. The active high TRUNAS is also inverted, to produce the active low MTT run = L signal (TRUNCA) for the MTT control logic. The *command (CMD) stop MTT* signal (TSTP6A), *master reset* signal (TXRS1B), the combination of input logic *forward direction* (FWD DIR)= H (TDIRIS) and *end of tape received* (EOT RCVD) (TEOTCO), or the combination of input logic *reverse direction* (REV DIR)= H (TDIRIR) and *beginning of tape received* (BOT RCVD) (TBOTCO) resets TRUNAS to low and TRUNCA to high. This disables the run logic in the MTT.

(2) *Tape direction indicators*. With the *MTT run = H* signal (TRUNAS) high when the *FWD DIR = H* signal (TDIRIS) goes high, the FORWARD indicator lights. When the *REV DIR=H* signal (TDIRIR) goes high, the REWIND indicator lights. The high *lamp test = H* signal (TLMPTO) lights both indicators.

5-18. Write Timing Counter (fig. 5-27 and 5-28). The write timing counter is a utility counter for the write control logic. The counter is started by one of three following signals: *write counter reset* (CTR RST) (TWRIRA), *longitude redundancy check counter reset* (LRC CTR RST) (TLRCRA), or *master reset* (TXRS 1B). The signal produces the active low *write timer set* signal (TCRS7A). Signal TCRS7A sets the *set=H/1-5* **µ***s = L* (TC70BQ), *set=H/5-10* **µ***s = L*

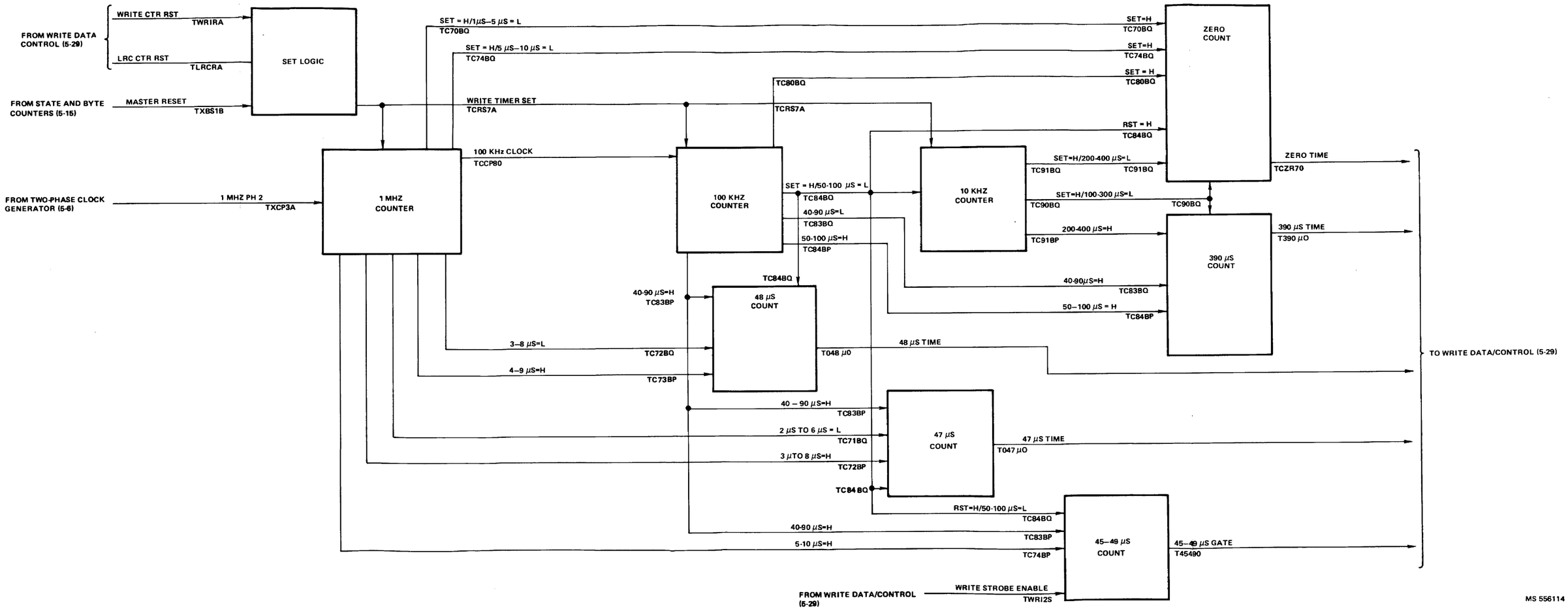

Figure 5-27. Write Timing Counter Block Diagram

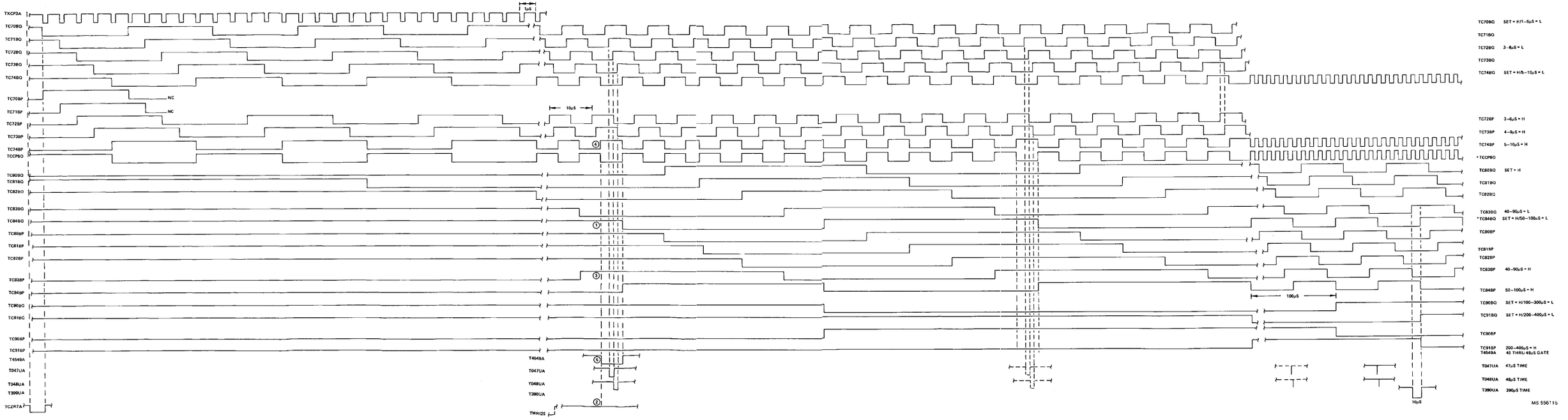

Figure 5-28. Write Timing Counter Timing Diagram

(TC74BQ), *set = H* (TC80BQ), *set = H/50-100 µs = L* (TC84BQ), *set = H/100-300 µs = L* (TC90BQ), and *set = H/200-400 µs = L* (TC91BQ) signals high. These high signals produce the zero time output signal (TCZR70). The next *1-MHz PH2** clock (TXCP3A) starts the count. The counter counts from 0 to 400 µs in 1-MHz steps. The desired timing is selected by a combination of counter signals. With the *40-90 µs = H* (TC83BP*), set = H/50-100 µs = L* (TCB4BQ), and *4-9 µs = H* (TC73BP) signals at a high level, when the *3-8 µs = L* signal (TC72BQ) goes high, the active high 40-es time output signal time (T048UO) goes high. With the TC83BP, TC84BQ, and *3-8 µs = L* (TC72BQ) signals at a high level, when the *26 µs = L* signal (TC71BQ) goes high, the active high 47Ds output signal (T047UO) goes high. When the counter is started by TWRIRA, the *write strobe* enable signal (TWRI2S) also enables the 45-to 49-µs count output. With TWRI2S, TC83BP, and TC84BQ at a high level, when the *5-10 µs = H* signal (TC74BP) goes high, the active high 45-49 Dis gate output signal (T45490) goes high. The active high 390Ds time output signal (T390UO) is produced when the TC90BQ, *200-400 µs = H* (TC91BP), and *50-100 µs = H* (TCS4BP) signals are at a high level and the *40-90 µs = L* signal (TCB3BQ) goes high.

5-19. Write Data Control Logic (fig. 5-29). The write data control logic is located in the card cage. Related switches and indicators are located on the front panel. The function of this logic is to provide signals that enable write heads in the MTT; provide timing for the interrecord gap, tape byte density, write request delay, and longitude redundancy check (LRC); provide gates for the file protect, latitude/longitude parity, and timeout errors; and provide gates for resetting the MTT write flip-flops write data drivers, and the strobe which eventually activates the data write heads in the MTT. The logic consists of the following:

Write enable latch
File protect error (FPE) detector
Write/erase delay counter (65/80 ms)
Latitude/longitude parity error detector
Write counter
Write data drivers
Write command timeout error detector
Write request delay counter
Longitude redundancy check (LRC) counter
Write flip-flops reset OR gate

a. Write Enable Latch (fig. 5-29). The write enable latch logic includes the WRITE ENABLE switch-indicator on the front panel. *Low no write = H* (TWRITP), *no erase forward* (ERS FWD) = H (TERSFP), *or erase reverse* (ERS REV) *latch = L* (TERSRP) signals produce the high write/ *erase = H* output signal (TWENCO). When the WRITE ENABLE switch on the front panel is set to on, the permanently low NAND gate pulldown signal is disconnected from the output signal. The write *enable switch (SW) = H* output signal (TWENA04) goes high. The high TWENA04, with the low *file protect = H* signal (XFPRSA), the high MTT *ready to receive* signal (TRDY10O), and the high on line set signal (TONLNS) produces the low *main timing counter (MTC) is write enabled* output signal (TRWE1A). Signal TRWEIA is inverted to provide the *MTC is write enabled* output signal (TRWE10). Signal TRWE10 goes to the front panel where it lights the WRITE ENABLE indicator. When the leading edge of the high 1-*MHz PH1* clock (TXCQ1B) occurs, the high TWENCO, TRWE1O, and volts to *read/write head* signal (TSNC1S) set the write enable latch output signal *write enable flipflop (FF)* (TWENOS) to high. Signal TWENOS also is inverted to eventually produce the low output signal MTT write *enable = L* (TWDBEB). The latch is reset by the combination of the high TSNC1S, the low TWENCO, and the next high clock TXCQ1B. The latch is also reset by a low TRWE10O or by a *low master reset* signal (TXRSOB). Signal TWENOS goes low and TWDBEB goes high when the latch is reset.

b. File Protect Error Detector (fig. 5-29). When the *write/erase = H* signal (TWENCO) and *main timing counter (MTC) is write enabled* signal (TRWE1A) are high (meaning write or erase is commanded and the MTC is not enabled), the *if FPE, erase/write inhibit = L* output signal (TFPE2A) goes low. If both TWENCO and TRWE1A are high, and the reset write *flip-flop* (FF) = H signal (TSNC2S) is high when the *1-MHz PH2* clock (TXCQ3B) goes high, the active low *set file protect error* output signal (TFPE1A) is produced.

c. Write/Erase Delay Counter (fig. 5-29 and 5-30). The delay created by the 65/80-ms write/erase delay counter makes up part of the interrecord gap time. This delay occurs just prior to the writing of data. The output starts the write counter. The start of this counter coincides with the completion of the start delay counter in the start/stop control at either 150 ms (initial start) or 40 ms (running start). When the write = H signal

(TWRITQ) is high and the *standing start or flying start delay* signal (TSTR90) goes high, the output *signal write start delay* (TWRQ1A) goes low. The counter has a set and reset function.

(1) *Reset (fig. 5-30).* The counter is reset by three separate signals; *master reset* (TXRSIB), forward end of tape interrupt (*FWD EOT INT*) (TINT7A), and TWRG1A (at completion of counter cycle).

(a) Master reset. When the *master reset* signal TXRSIB goes low, the *write/erase delay counter is reset* (WR/ERS DLY CTR is RST) = H signal (TWRG2R) goes high and internal signal TWRGOS goes low. The low TWRGOS causes internal signal TWRGIR to go high. With TWRG1R high, the next *1-MHz PH1* clock (TXCQ1B) produces internal signal TWRG3A. Signal TWRG3A can reset TWRG2R to high, but in this case it is already high.

(b) FWD EOT INT. The low *FWD EOT INT* signal (TINT7A) resets TWRGOS to low. The low TWRGOS resets TWRG1R to high. The next TXCQ1B clocks out the low TWRG3A and resets TWRG2R to high.

(c) *TWRG1A*. At the completion of the counter cycle, the internal signal TWRG2S is high. With TWRG2S high, the next high *1-MHz PH2* clock (TXCQ3B) produces the active low internal signal TWRGIA. The low TWRG1A resets TWRGOS to low. The low TWRGOS resets TWRG1R to high. With TWRGIR high, the next *1-MHz PH1* clock (TXCQIB) produces TWRG3A. The low TWRG3A resets TWRG2R to high and TWRG2S to low.

(2) *Set (fig. 5-30).* When *the standing start or flying start delay* signal (TSTR90) goes high as a result of the *1-MHz PH1* clock (TXCQ1B) and either the *no write = H* (TWRITP) or the *no erase forward* (FWD) = H (TERSFP) signal is low, the low internal signal TWRGOA is produced. The low TWRGOA sets internal signal TWRGOS to high. Signal TWRGOS enables TWRG2A. A simultaneously high TWRG1R produces the *65-ms write (WR)/80-ms erase delay (ERS DLY)* signal (TWRGRA) which resets the main time counter. The *zero time* signal (TCZROO) goes high and with TWRGOS and TXCQIB both high, produces a low TWRG2A. The low TWRG2A sets TWRGIR low and TWRG1S high. When the command is write, *write = H* signal (TWRITQ) is high. When TWRG1S is also high and the *65-ms time* signal (T075MO) goes high, the next *1-MHz PH1* clock (TXCP1B) clocks out the *65-ms write delay (WR DLY)= L* output signal (TWRG6A). At the same time the *write/erase* delay bit 2 signal TWRG2S is set to high and *the write/erase delay counter is reset* (WR/ERS DLY CTR is RST) = H signal (TWRG2R) is set to low. When the command is erase, while TWRG1S and the *80-ms time* signal (T080MO) is high, the next high TXCQ1B produces the low TWRG4A. The low TWRG4A sets TWRG2R to low and TWRG2S to high.

d. Latitude/Longitude Parity Error Detector (fig. 5-30). During the write command when the write = H signal (TWRITQ) is high, if either a lateral or longitudinal parity error exists--*set lateral parity* signal (TLATSA) or *set longitudinal* signal (TLNGSA), respectively--the active low *write parity error signal* (TWPE0A) is generated.

e. Write Counter (fig. 5-29 and 5-31). The write counter provides the spacing in time that determines the recording density on the tape. The counter provides a strobe after the initial delay and recycles continuously to provide a strobe to write each byte at 50-ms intervals until there is no more data. On the cycle where there is no more data, the counter stops. The counter functional description is divided into the reset and set functions.

(1) Reset. The counter is stopped by any one of five low signals that activate the reset. When the reset is activated, the *65 ms sets latch =H* signal (TWR10S) is reset low and *write counter is reset* (WR CTR is RST) = H signal (TWRIOR) is reset high. The five signals that activate resets are as follows:

(a) Read/write (R/W) start delay latch = H (TRENIS)

(b) Write parity error (TWPE0A)

(c) Write command data parity error (PE) (TXDPEA)

(d) Master reset (TXRS0B)

(e) TWR11A

Signal TWR11A goes low when there is no more data as indicated by the six high input signals; *input data buffer full = L* (TDBFBP), *request buffer full latch = L* (TRBFBP), *write for longitude redundancy check (LRC) = H (TLCC0S), write/erase delay is reset (WR/ERS DLY is RST)=H* (TWRG2R), TWRIIR, and TXCQ1B.

(2) *Set*. At the completion of the 65-ms write delay, TWRG6A goes low. This sets TWRIOS to high and TWRIOR to low. The write counter continues as long as TWRI0S is high. Initially, TWRI2R and TWRI3R are both high. When

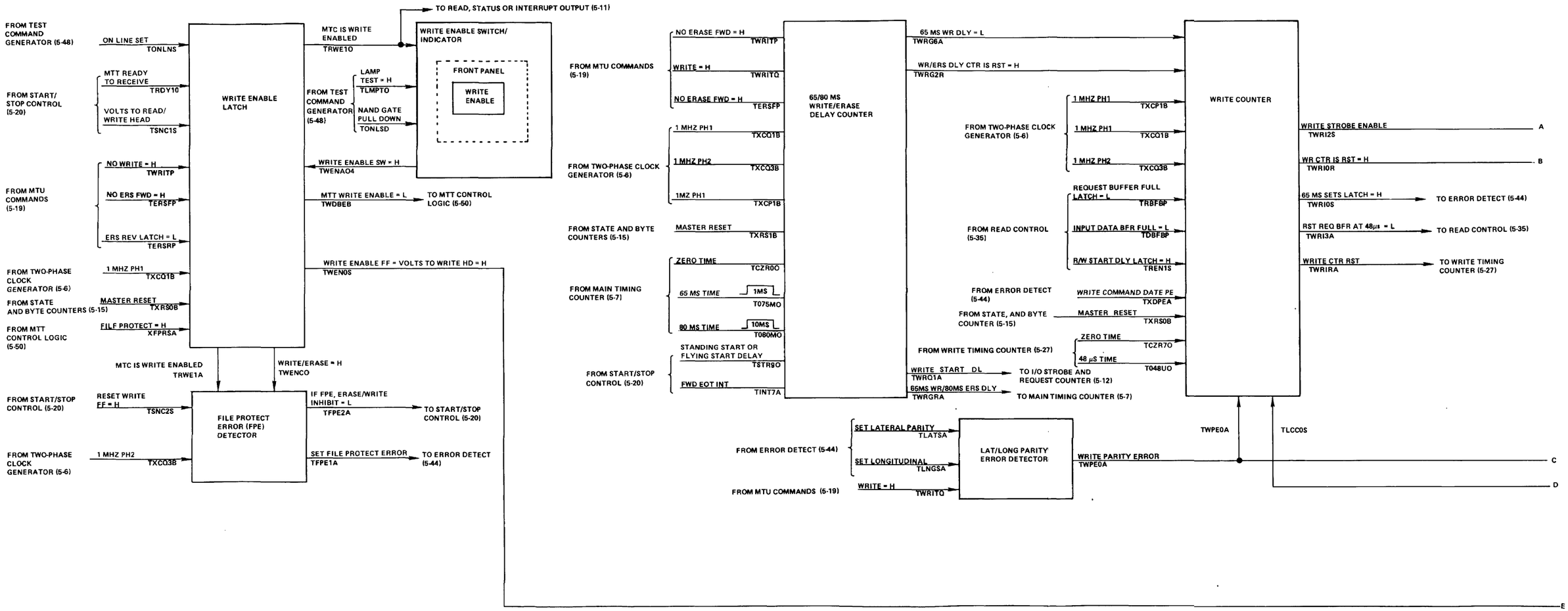

Figure 5-29. Write Data/Control Block Diagram (Sheet 1 of 2)

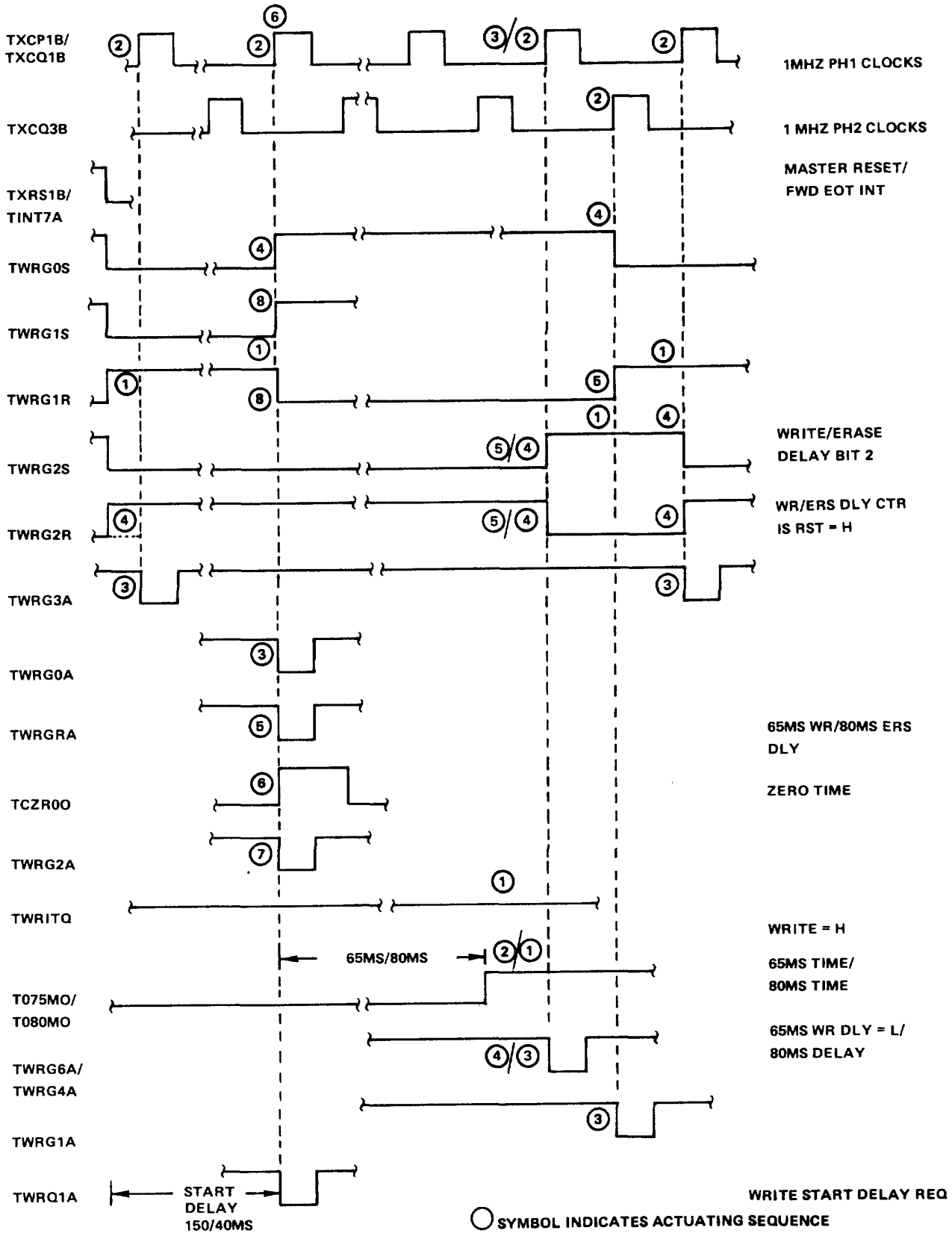

Figure 5-30. 65/80 MS Write/Erase Delay Timing Diagram.

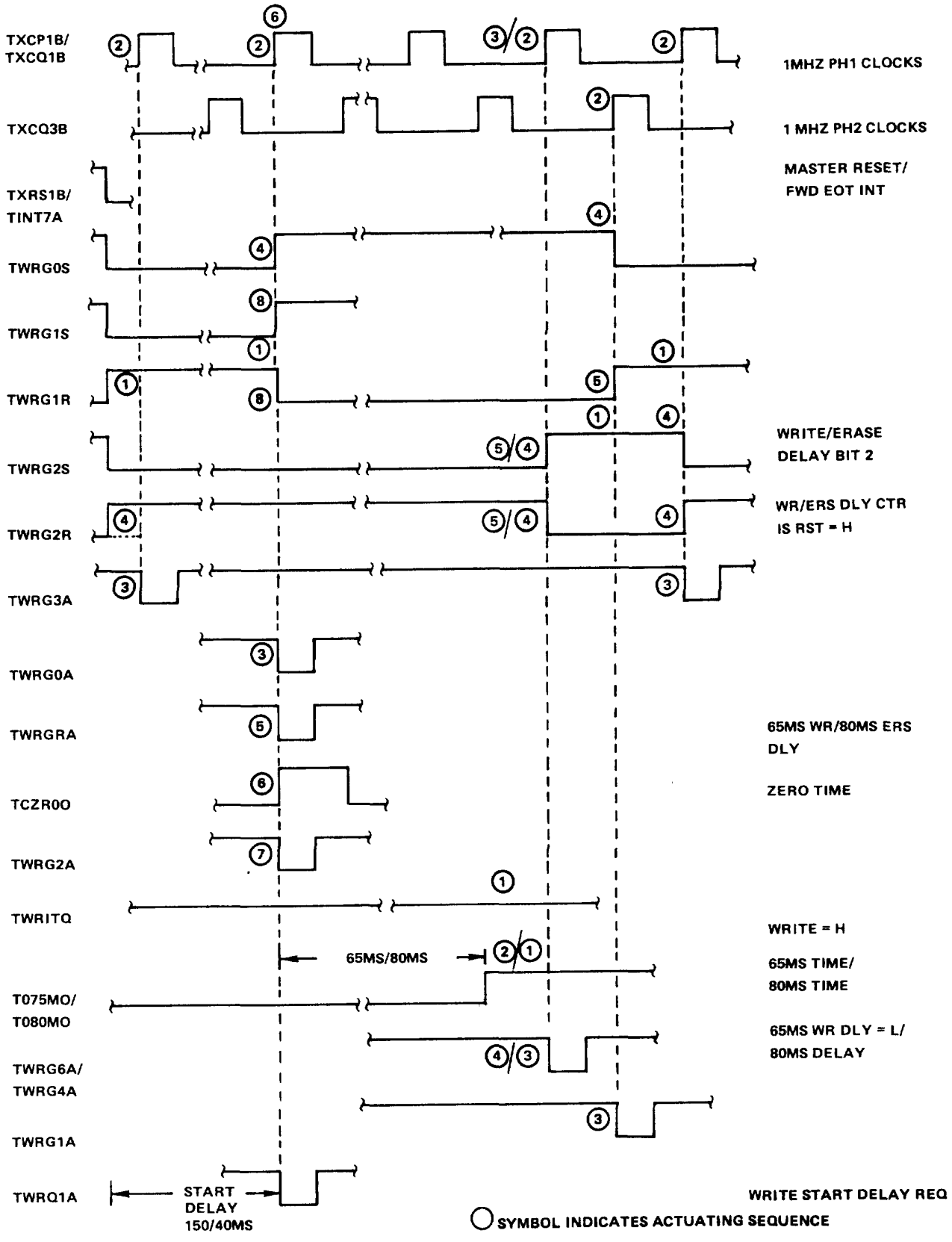

Figure 5-30. 65/80 MS Write/Erase Delay Timing Diagram.

TWR1OS also goes high, the next TXCQ3B pulse produces the low TWR12A. On subsequent cycles, TWR1OS TWR12R, and TWR13R go high. The next TXCQ3B pulse produces the low TWR12A. Signal TWR12A sets TWR11S to high and TWR11R to low. The high TWR11S and TWR12R produce the low write counter resets (CTR RSTS) timer output signal (TWR1RA). Signal TWR1RA goes to the write timing counter where it resets the timer count to zero. The zero time signal (TCZR70) goes high and, with TWR11S high, the next TXCP1B pulse produces the low TWR14A. The low TWR14A sets TWR12S high and TWR12R low. With TWR12S high, when the 48ps time signal (T048UO) goes high, the next TXCP1B pulse produces the low TWR16A. The low TWR16A sets TWR13S to high and TWR13R to low. A high TWR13S marks the end of one byte writing cycle and the beginning of another. With TWR13S high, the next TXCQ3B pulse produces the low output signal reset request buffer at 48 ps (RST REQ BFR at 48 ,is)=L (TWR13A). The low TWR13A resets TWR11R to high and TWR11S to low. The low TWR1 1S resets TWR12S to low and TWR12R to high. With TWR12R high, the next TXCQ1B pulse produces the low TWR15A, which resets TWR13S to low and TWR13R to high. With TWR12R and TWR13R high, the next TXCQ3B pulse produces TWR12A, which sets TWR11S high for the time zero signal for the next byte. The write counter continues to cycle every 50 ,us until the low TWR13A resets the request buffer in the read control logic and no more data is received.

f. Write Data Drivers (fig. 5-29). When the write counter reset (CTR RST) signal (TWR1RA) of the write counter resets the write timing counter to 0, 45 ,is later the 45-49 'Is gate signal (T45490) goes high for 5 Its During this 5 its eight active high= 1 write data with parity bits TROOBQ through TR07BQ and TROPBQ) are gated to the MTT as active low= I MTT write (WR1 data with parity signals (TWDBOA through TWDB7A and TWDBPA). The write data is present at the MTT for 5 ILs With TWR12S high during the 5 'is, the 47-is time signal (T047UO) goes high. This produces the active low write strobe signal (TWDBSA), that causes the write head to be energized for each logical one in the byte.

g. Write Command Timeout Error Detector (fig. 5-29). If there is a' low IIO data sync signal (TWR11A) or if the request buffer is not full as indicated by a low request buffer full latch = H signal (TRBFBQ), when the 1-MHz PH2. clock (TXCP3B) 5-158 and the 47-;is time signal (T047UO) both go high at about the same time (see figure 5-28 for timing of TXCP3B and T047UO), the data not ready = timing error=L output signal (TWTOCA) is generated if the following conditions also exist.

(1) Power is on (on line set signal (TONLNS) is high)

(2) Write is the command (write=H signal (TWR1TQ) is high)

(3) LRC counter is not set (LRC CTR RST=H signal (TLCCOR) is high)

(4) Write data enable strobe is enabled (TWR12S is high)

h. Write Request Delay Counter (fig. 5-29 and 532). The output of the write request delay counter logic is the write request for more data. The output is delayed by the counter for 7 ,is after the current input data from the ADP is enabled. The enabled ADP is indicated by a low I/IO data synchronizer (SYNC) signal (TWR1IA). Initially, the master reset signal (TXRSOB) sets the counter enable=H signal (TWR1CP) to low. This resets and inhibits the other flip-flops of the counter. At the completion of the counter cycle, TWR13P goes high and clocks signal TWR1CP to low. When TWR11A goes low, it resets TWR1CP to high, enabling the counter. The counter is clocked by the 1-MHz PHI clock (TXCP1B). When TWR12P goes high at 6.5 tis the next 1-MHz PH2 clock (TXCO3B) (7 'is from TWR11A) clocks out the write request delay (TWR1OA) if the following conditions exist.

(1) Write is the command (write=H (TWR1TQ) is high)

(2) Input/output timing error (IIO timing error=L (TTMERP) is high)

(3) LRC counter is reset (LRC CTR RST=H (TLCCOR) is high)

i. LRC Counter (fig. 5-29 and 5-33). When an EOB is received with the block counter equal to zero, a write terminate operation is initiated. The write terminate operation consists of encoding and writing the longitudinal redundancy check (LRC) character. The encoding and writing consists only of resetting the write flip-flops at the completion of a 390-ps delay. If the total number of logic l's written in the same bit position for all the bytes in all the blocks for this write command is an odd number, the write flip-flop in the MTT changes its output state when reset. With an odd number of bits, a change of state writes a logic 1 for that bit

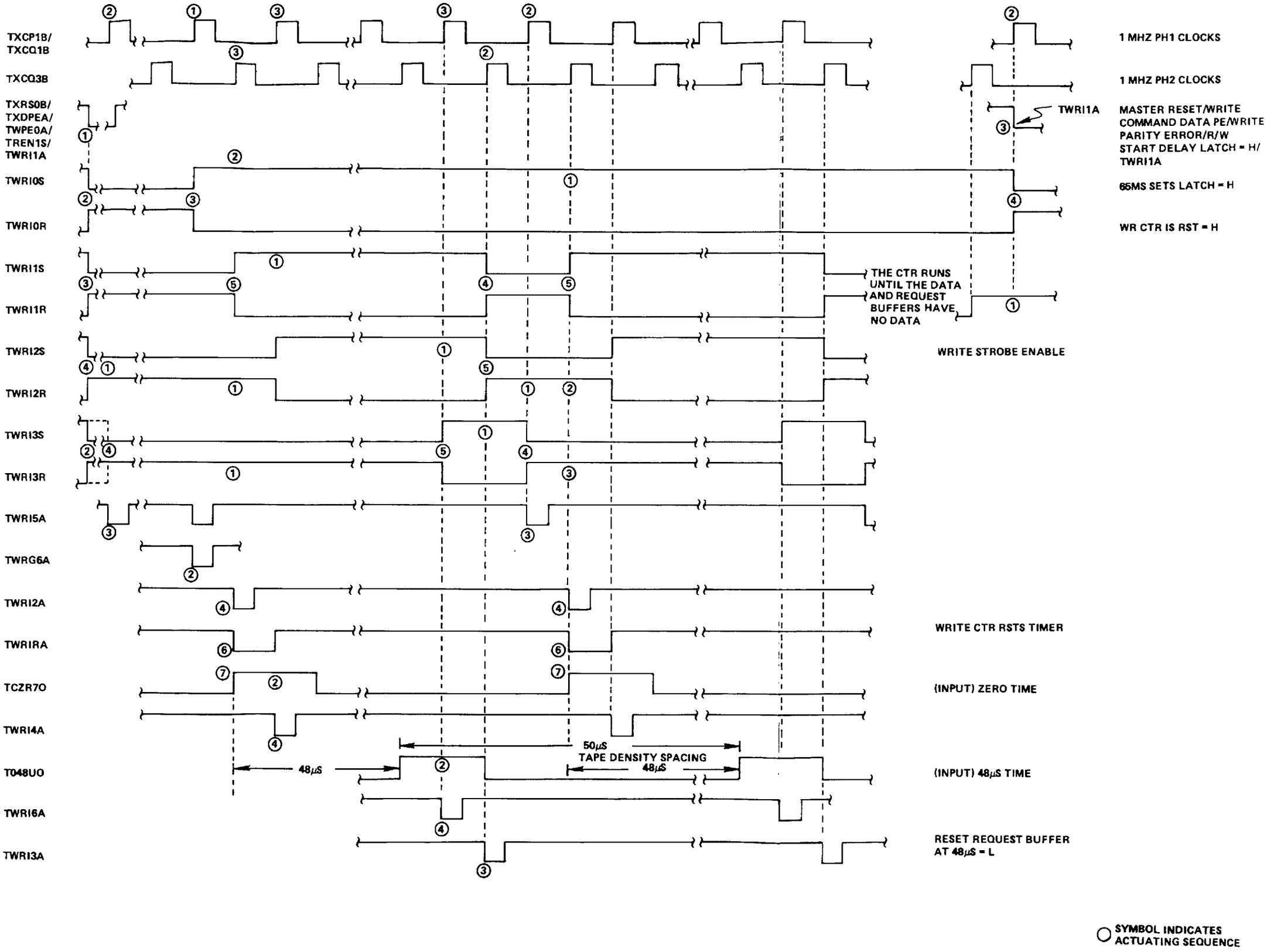

FIGURE 5-31. Write Counter Timing Diagram.

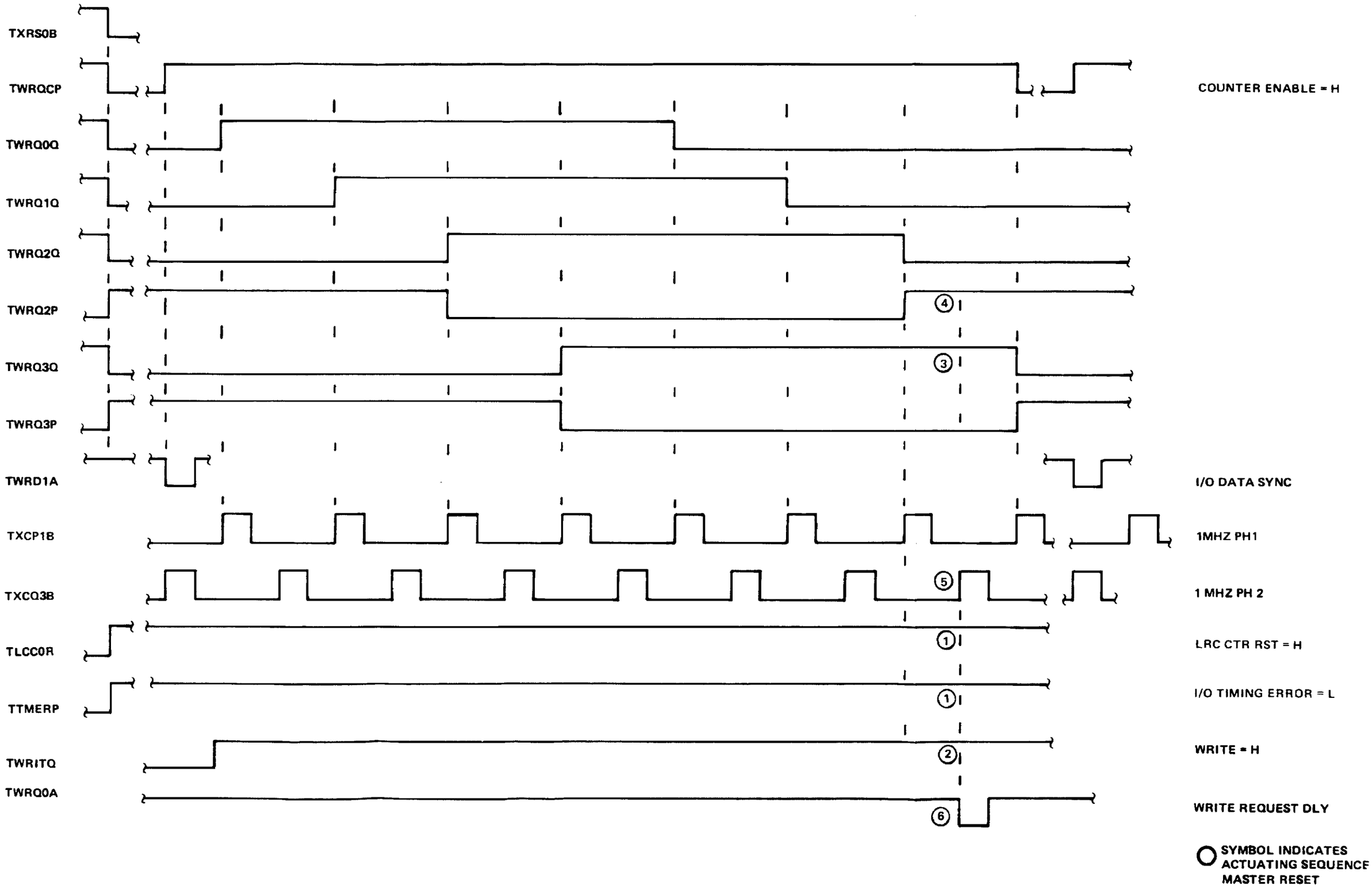

FIGURE 5-32. Write Request Delay Counter Timing Diagram.

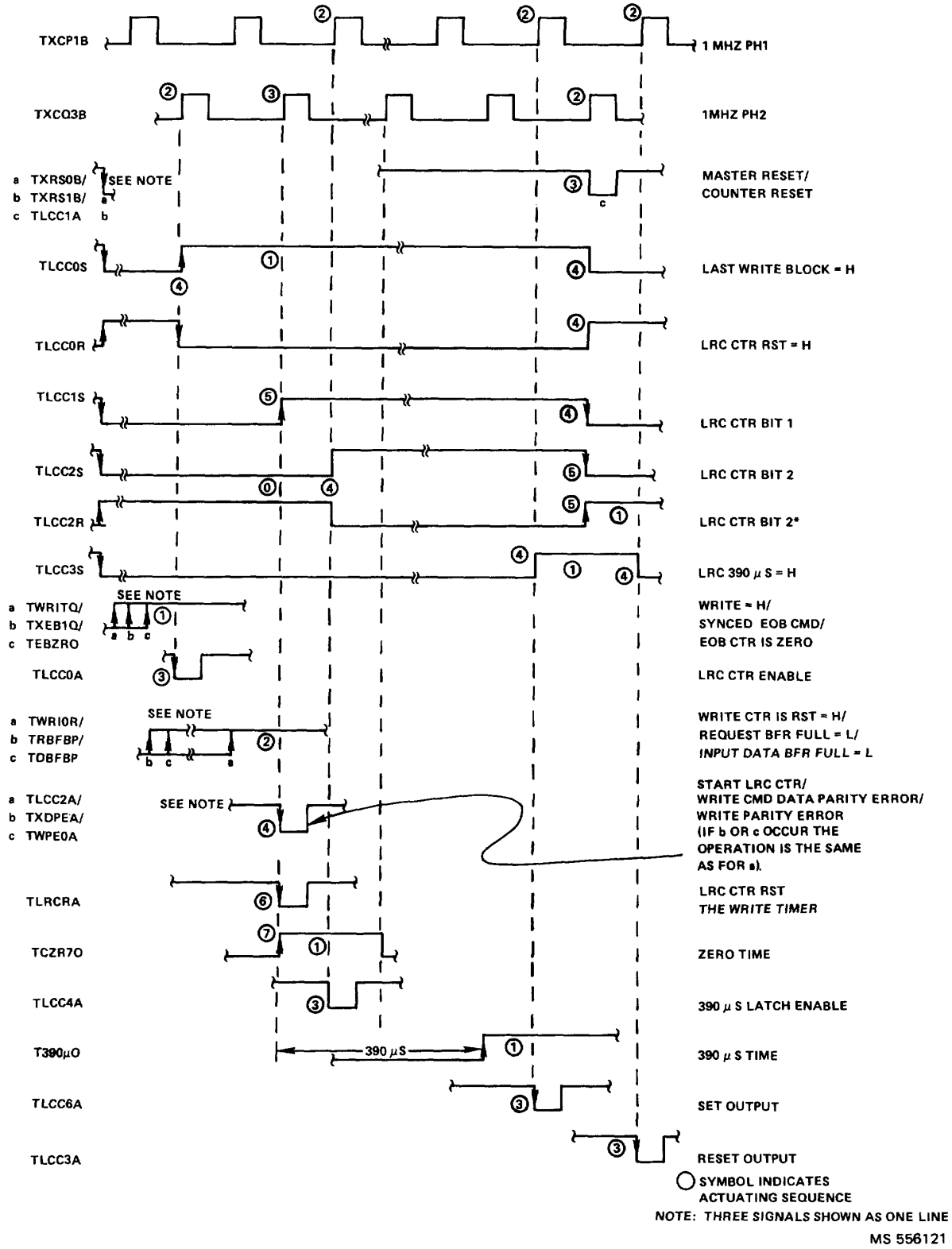

Figure 5-33. LRC Counter Timing Diagram.

position. The 9-bit (including parity) LRC character is therefore written with l's for odd totals and O's for even totals. The LRC character is read as it is written and is used to clock the LRC register in the error detect logic. If there is a discrepancy between the read and write character, an error is detected. The LRC counter is reset initially by the master reset signals (TXRSOB and TXRS1B). Signal TXRS1B resets the last write block=H (TLCCOS) and LCR counter (LRC CTR) bit I (TLCC 1S) signals to low and the LRC counter is reset (LRC CTR RST) = H signal (TLCCOR) to high. The low TLCCIS resets the LRC CTR bit 2 signal (TLCC2S) to low. Signal TXRSOB resets the LRC 390 CIs=H output signal (TLCC3S) to low. When the three input signals write=H (TWRITQ), syncronized end of block command (SYNCED EOB CMD) (TXEB1Q), and end of block counter (EOB CTR) is zero (TEBZRO) are high, the next 1-MHz PH2 clock (TXCQ3B) produces the low TLCCOA. The low TLCCOA sets TLCCOS to high and TLCCOR to low. Signal TLCCOS is used to partially satisfy the logic to reset the write counter. When the write counter resets, it provides the write counter (CTR) is reset (RST)=H signal (TWRIDR) to the LRC counter. With TLCCOS TWRIOR, TRBFBP, and TDBFBP high, the next TXCQ3B produces the low TLCC2A signal. The low TLCC2A sets TLCC1S to high in order to produce the low output signal LRC counter reset (CTR RST) (TLRCRA). Signal TLRCRA resets the write timing counter to zero, thereby producing the zero time signal (TCZR70). With TCZR70 high, the next 1-MHz PHI clock (TXCP1B) produces the low internal 390-1xs latch enable signal (TLCC4A). Siqnal TLCC4A sets the internal LRC counter (CTR) bit 2 signal (TLCC2R) to low and TLCC2S to high. With TLCC2S high, when the 390-es time signal (T390UO) goes high, the next TXCP1B produces the low internal set output signal (TLCC6A). Signal TLCC6A sets the LRC 390 Ks=H output signal (TLCC3S). With TLCC3S high, the next TXCQ3B produces TLCC1A. Signal TLCC1A resets TLCCOS and TLCC1S to low and TLCCOR to high. The low TLCCIS resets TLCC2S to low and TLCC2R to high. With TLCC2R high, the next TXCP1B produces the low TLCC3A signal. Signal TLCC3A resets the output signal TLCC3S to low. This completes the LRC counter cycle.

j. Write Enable OR Gate (fig. 5-29). The LRC 390 pts = H (TLCC3S), reset (RST) write flip-flop (FF) = L (TSNC2R), or low write enable flip-flop (FF) (TWENOS) signals (low indicates read command) 5-164 produce the write flip-flop (FF) RST=L output signal (TWLRCA).

5-20. Read Data Logic (fig. 5-34). The read data logic is located in the card cage. The logic consists of line receivers, register reset logic, and the 9-bit read register. The line receivers receive data bits from the MTT. The low L=read data with parity signals (XRDBOA through XRDB7A with XRDBPA) and the L = read strobe signal (XRDBSA) are inverted by the line receivers to produce the high signals H=read data with parity (TROBOO through TROB70 with TROBPO) and the H=read data strobes signals (TTCPOO and TTCPO1). Signals TTCPOO and TTCP10 clock the data through the register. The register generates the active high read data. with parity=H signals (TTOOBQ through TT07BQ with TTOPBQ) and the active low read data with parity = L signals (TTOOBP through TTO7BP with TTOPBP). Signals TTOOBP through TT07BP with TTOPBP go high, and TTOOBQ through TT07BQ with TTOPBQ go low when the low clear read register read command (TTRSCA), read enabled by start delay=H (TRENOS), or low speed=H (TSPNIR) signals produce the low reset signals (TTRSOA and TTRSlA).

5-21. Read Control Logic (fig. 5-35 and 5-36). The read control logic is located in the card cage. At the completion of the tape start delay, a data byte is read from the tape. The read control logic then provides a read request signal to the ADP through the MTU I/O strobe and request counter logic and I/ O interface logic. At the same time, the read control logic generates control strobes that move the byte into the read, status, or interrupt output logic for transfer when the responding enable signal is received from the ADP through the MTU I/O interface logic and the address, command, and enable logic. Also, in response to the enable, the read control logic generates the read request signal for the next byte of read data delayed about 7.5 Is The read request signal is generated and transferred to the ADP. At the same time, the first byte is moved into the read, status, or interrupt output logic for transfer to the ADP. When the enable is received from the ADP, the byte is transferred to the ADP and a new 7.5-,us delay is generated. The cycle continues until, with the end of block (EOB) counter decremented to zero, an end of block command (CMD) resets the logic. The read control logic is organized by functional blocks on figure 5-35. The

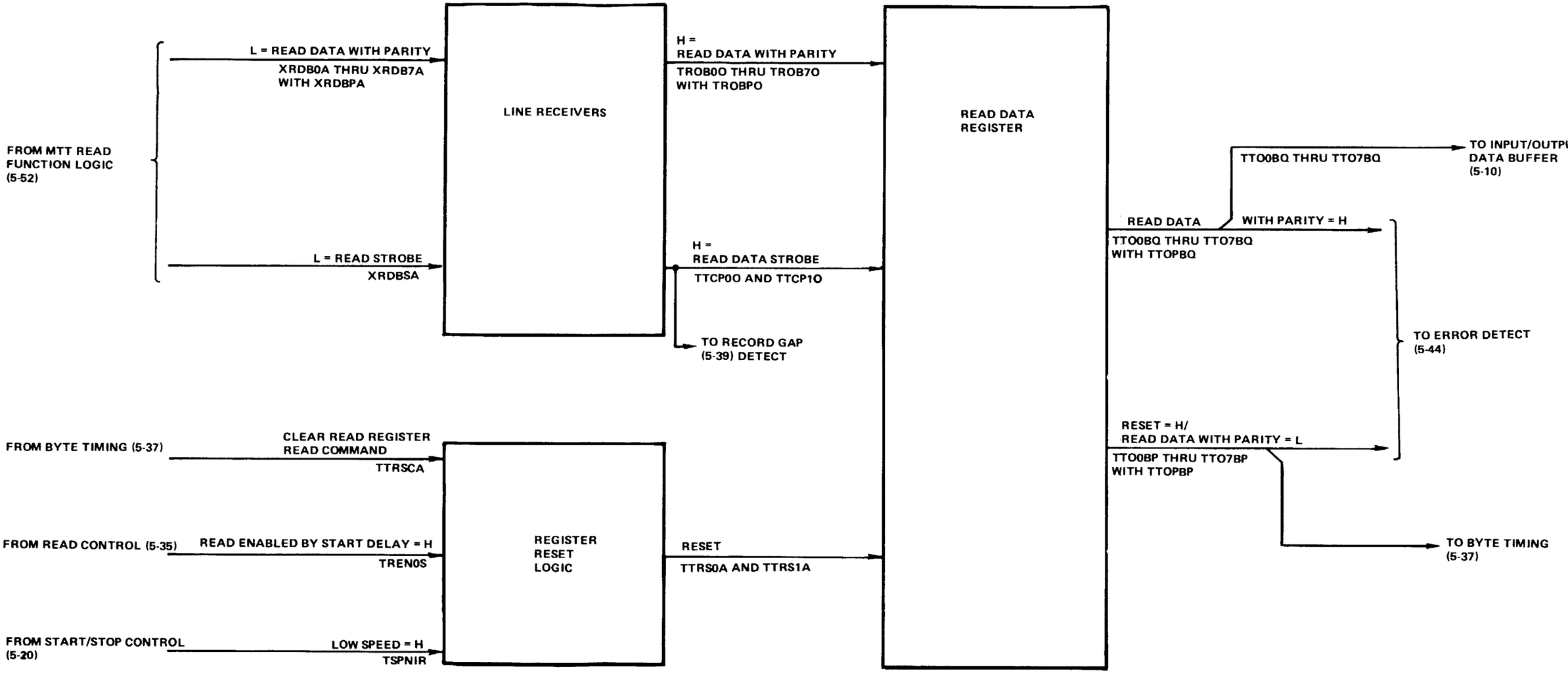

FIGURE 5-34. Read Data Block Diagram.

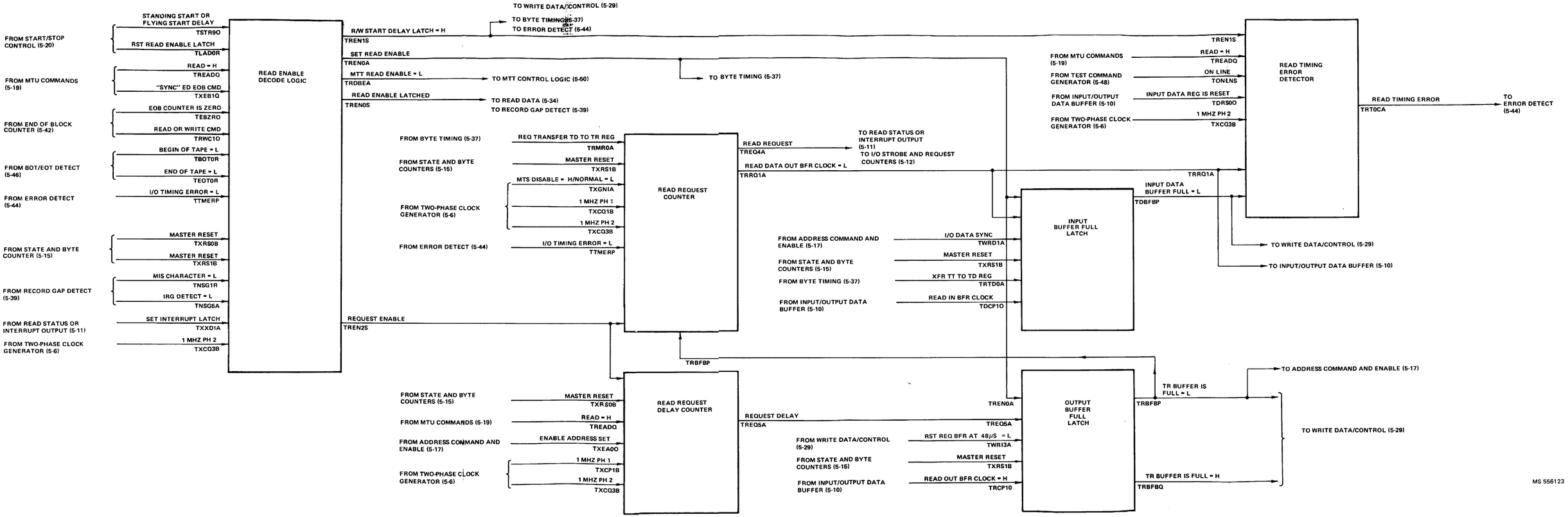

FIGURE 5-35. Read Control Block Diagram.

timing for subsequent requests after the initial request is shown in figure 5-36. The logic is described in the following subparagraphs.

a. Read Enable Decode Logic. The high standing start or flying start delay signal (TSTR90) produces the low set read enable output signal (TRENOA). Signal TRENOA also sets the read enable latched output signal (TRENOS) to high. Signal TRENOS is also inverted to produce the low MIT read enable= L output signal (TRDBEA). At the same time, the high TSTR90 and the high read or write command CMD signal (TRWC10) provides the signal that sets the read/write (RIW) start delay latch=H (TREN1S) and request enable (TREN2S) signals to a high level. Signal TREN1S enables the read timing error logic. Signal TREN2S enables the read request counter and the read request delay counter. Signals TREN1S and TREN2S are reset low when the last block of data has been read, as indicated by the high syncronized end of block command (SYNCED-EOB-CMD) (TXEB 1Q) and end of block (EOB) counter is zero (TEBZRO) signals. With the read=H (TREADQ), TXEB1Q, and TBBZRO signals at the high level, when the I-MHz PH2 clock (TXCQ3B) goes high, the reset is executed. Signal TREN1S is also reset low by the following signals: begin of tape=L (TBOTOR), end of tape=L (TEOTOR), low I/IO timing error (TTMERP), missing (MIS) character= L (TNSG 1R), or low master reset (TXRSOB). Signal TREN2S is also reset low by the interrecord gap (IRG) detect = L (TNSG5A), set interrupt latch (TXXDIA), or master reset (TXRSOB) signals.

b. Read Request Delay Counter (fig. 5-35 and 536). The counter provides a delay of about 7.5 tus between receipt of the enable and generation of the read request for the next enable. The master-reset signal (TXRSOB) sets the internal flip-flop (FF) reset signal (TREQCP) low. Signal TREQCP resets the counter flip-flops. When the read=H (TREADQ) and request enable (TREN2S) signals are high, and the enable address set signal (TXEAOO) goes high, TREQCP goes high and causes the counter to start. The next 1-MHz PHI clock (TXCP1B) starts the count. With TREQ2P and TREQ3Q high, the seventh 1-MHz PH2 clock (TXCQ3B) produces the request delay output signal (TREQ5A). Signal TREQ5A is produced 6.5 rs after the counter starts and up to 7.5 ,us after the enable.

c. Output Buffer Full Latch (fig. 5-35 and 5-36). The output buffer full latch is used for read and write functions. The timing in figure 5-36 is for the read function. The high transfer request (TR) buffer is full=H signal (TRBFBQ) and low TR buffer is full=L signal (TRBFBP) indicates that read or write data is in the output buffer of the input/ output data buffer logic. Initially, for either the read or write command, the set read enable signal (TRENOA) resets the output signal TRBFBP to high and TRBFBQ to low.

(1) Write function. For the write function, when the first write data byte is clocked into the output buffer of the input/output data buffer logic, the read out buffer (BFR) clock = H signal (TRCP 10) produces high output signal TRBFBQ and low output signal TRBFBP (TR = output). When the write data byte is written on tape, the reset request buffer (RST REQ BFR) at 48 ,us = L signal (TWRI3A) resets the latch outputs (TRBFBQ is low and TRBFBP is high). The write cycle just described continues for each byte until the end of all blocks.

(2) Read function. For the read function, after the initial reset by TRENOA, the first byte of read data is read from the tape, and the read request signal (TREQ4A) is produced when three conditions are fulfilled as follows: the byte is clocked into the output buffer of the input/output data buffer logic by TRCP10; TRBFBQ and TRBFBP are set low; and the read request counter is inhibited. In response to the TREQ4A generated by the first read data byte, an enable is received from the ADP, causing the transfer of the first read data byte to the ADP. This results in the request delay signal (TREQ5A) being delayed about 7.5 ,us The delayed TREQ5A resets TRBFBQ to low and TRBFBP to high. A high TRBFBP enables the read request counter for the next byte. This cycle for read data continues until the output of the read-requestdelay counter is disabled by a low TREN2S. Latch output TRBFBQ is reset to low and TRBFBP is set to high by the master reset signal (TXRS1B).

d. Read Request Counter (fig. 5-35 and 5-36). This block of logic generates the read request signal and the read data out buffer (BFR) clock =L signal (TRRQ1A) that ultimately clocks the read data out of the output buffer of the input/output data buffer. Initially, master reset signal (TXRS1B) resets internal signal TRRQOQ to low. When the first data byte is read from the tape, the low request transfer timing decode to transfer request register (REQ transfer TDto-TR-REG) signal (TRMROA) sets TRRQOQ to high (TD is input and TR is output). With internal signals TRRQOQ and TRBFBP high, the next

1-MHz PH2 clock (TXCQIB) produces the high internal signal TRRQiP. With the request enable (TREN2S), I/O timing error=L (TTMERP), and TRRQ 1P signals all high, the next 1-MHz PH2 clock (TXCQ3B) produces the read request output signal (TREQ4A). This signal is sent to the ADP through the I/O strobe and request counter and the I/O interface logic. Signal TREQ4A also goes to the read, status, or interrupt output logic where it sets a latch that allows the enable from the ADP to transfer the data from the read, status, or interrupt output logic to the I/O interface. At the same time, with TRRQ1P high, TXCQ3B produces the read data out buffer (BFR) clock=L output signal (TRRQiA). Signal TRRQIA goes to the input/ output data buffer where it produces TRCP10. Signal TRCP10 clocks the data out of the buffer to the reads, status, or interrupt output logic. Signal TRCP10 also produces the low TRBFBP from the output buffer full latch function. The positive-going trailing edge of TRRQ1A clocks the MTS disable=H/normal=L signal (TXGN1A) into the readrequest counter. This causes TRRQOQ to be reset to low. When the enable is received from the ADP, the first byte is transmitted to the ADP, and TRBFBP goes high after a 7.5-ets delay. The time allowed for the ADP to respond to a request with an enable is 240 ns minimum to 22 tus maximum. The data bytes are written on the tape at 50-ts intervals; therefore, the enable is normally received before the next data byte is read from the tape. When the second byte of data is read from the tape, TRMROA goes low, and sets TRRQOQ high. With TRRQOQ and TRBFBP high, the next TXCQ1B produces a high TRRQ1P. This produces a high read request signal (TREQ4A) on the next TXCQ3B. At the same time that TREQ4A for the second byte is generated, TRRQiA for the second byte is also generated. This cycle continues for each read byte until the signals TREN1S and TREN2S from the read enable decode logic function are reset low.

e. Input Buffer Full Latch (fig. 5-35). The latch indicates when data (either read or write) is in the input buffer. Initially, the latch is reset for either read or write functions by the set read enable signal (TRENOA). When reset, the input data buffer full = L signal (TDBFBP) is high. The master reset signal (TXRS1B) also resets TDBFBP to high.

(1) Write function. The signal that clocks write data into the input buffer of the input/output data buffer is the read in BFR clock signal (TDCP01). Signal TDCP10, when high, sets TDBFBP to low. When the enable for the write 5-170 function is received from the ADP, the IIO data sync signal (TWRD1A) goes low. This resets TDBFBP to high. The cycle continues for all write data bytes.

(2) Read function. The signal that transfers read data into the input buffer of the input/output data buffer is the transfer transmit timing to timing decode register (XFR TT to TD REG) signal (TRTDOA). Signal TRTDOA also sets the latch output TDBFBP to low. When the read data out buffer (BFR) clock = L signal (TRRQ1A) goes low, it resets TDBFBP to high.

f. Read Timing Error (fig. 5-35). With three input signals high, when the input data buffer full=L signal (TDBFBP) goes low, the next 1-MHz PH2 clock (TXCQ3B) produces the read timing error signal (TRTOCA). The three input signals are as follows:

(1) On-line (TONLNS)

(2) Read=H (TREADQ)

(3) Input data register (REG) is reset (TDRS0O)

5-22. Byte Timing Logic (flg. 5-37 and 5-38). The byte timing logic is located in the card cage. The function of this logic is to provide the synchronous transfer of the read data byte from the tape to the output buffer of the input/output buffer. Then it is transferred through the I/O interface to the ADP. The byte is also read for the write function but not transferred to the input/output data buffer. The sequence of transfer signals is controlled by the byte timing counter. The counter is synchronized to the phase one clock. The transfer signals are a function of the count. The output of the transfer signals is synchronized to the phase two clock.

a. Byte Timing Counter (fig. 5-37 and 5-38). The byte timing counter is reset by the master reset signal (TXRS1B). Signal TXRS1B sets internal signal TKA00P to low. The low TKA00P resets the counter flip-flops and inhibits the counter. When any one of the read data with parity signals (TTO0BP through TTO7BP with TTOPBP) go low (indicating a bit has been read from the tape in either the read or write function), the internal signal TKRS0A goes low, resetting TKAOOP to high. When TKA00P goes high, the inhibit is removed from the counter and the next 1-MHz PH2 clock (TXCQIB) starts the counter. The time for latitude (LAT) parity test=H signal (TKA01Q) goes high on the first clock pulse. The input transfer (XFR) to outputlclear read register (CLR RD REG) signal (TKA01P) is produced by the third TXCQ1B clock

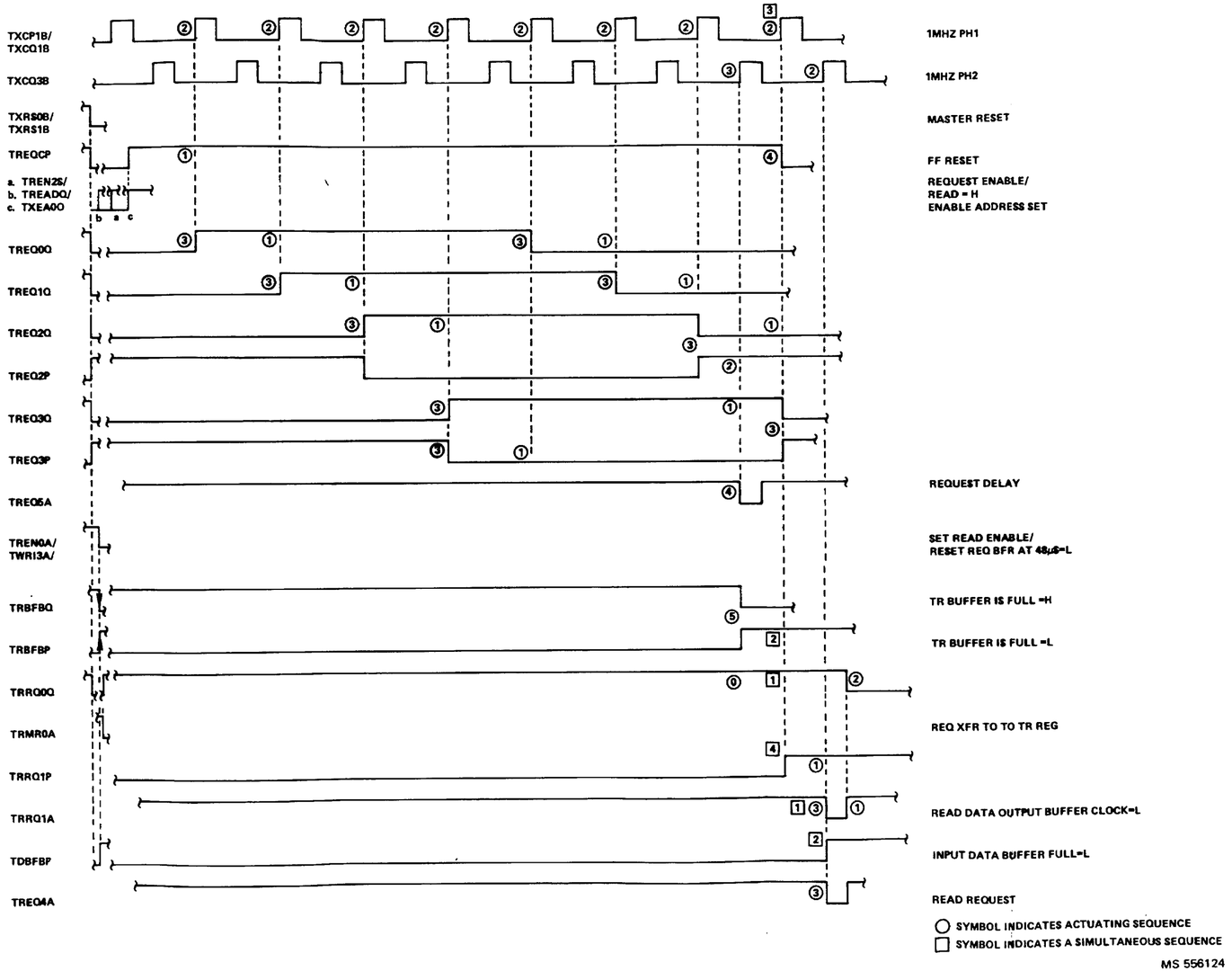

FIGURE 5-36. Read Request Timing Diagram.

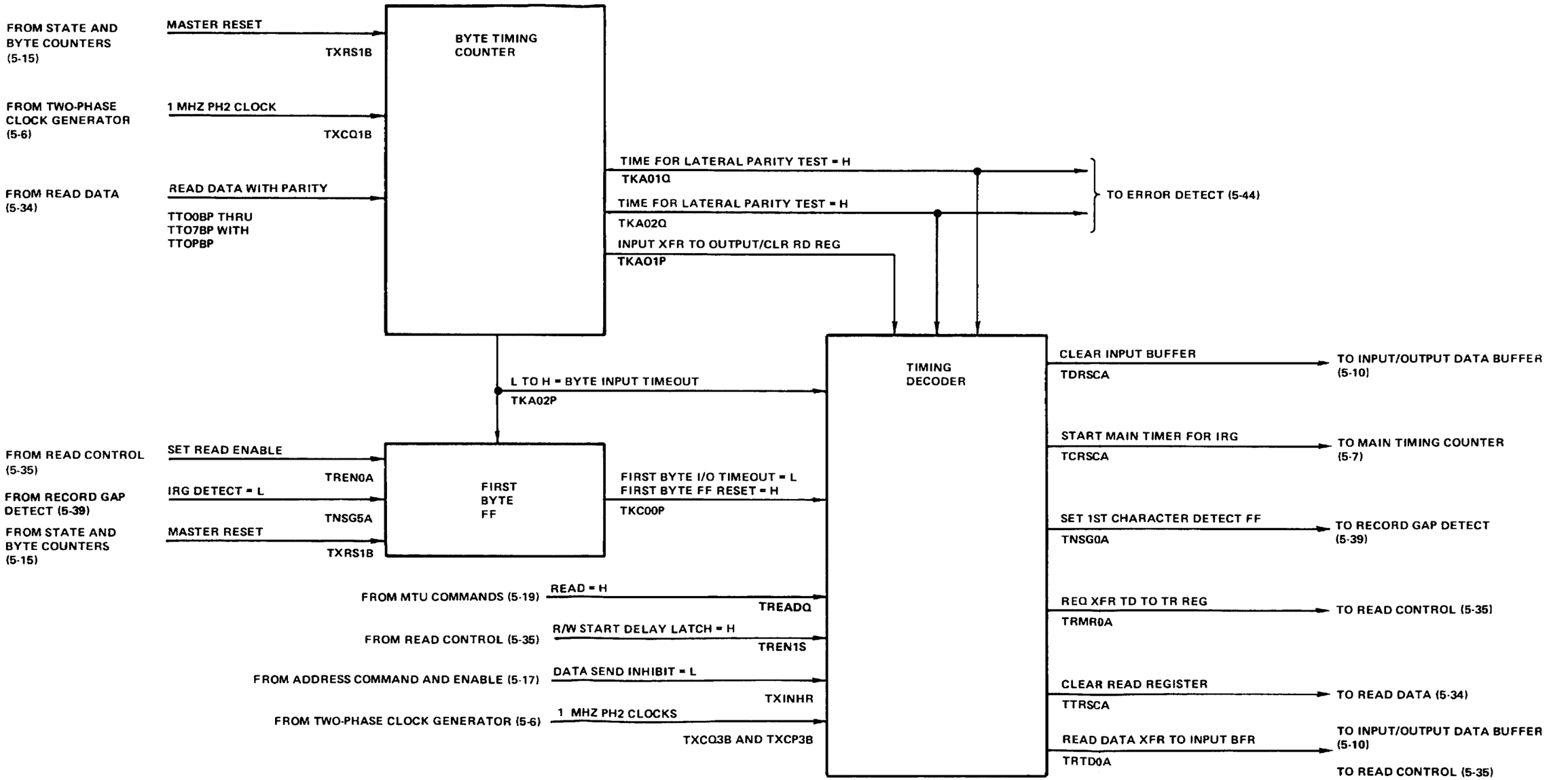

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Figure 5-37. Read Byte Timing Block Diagram

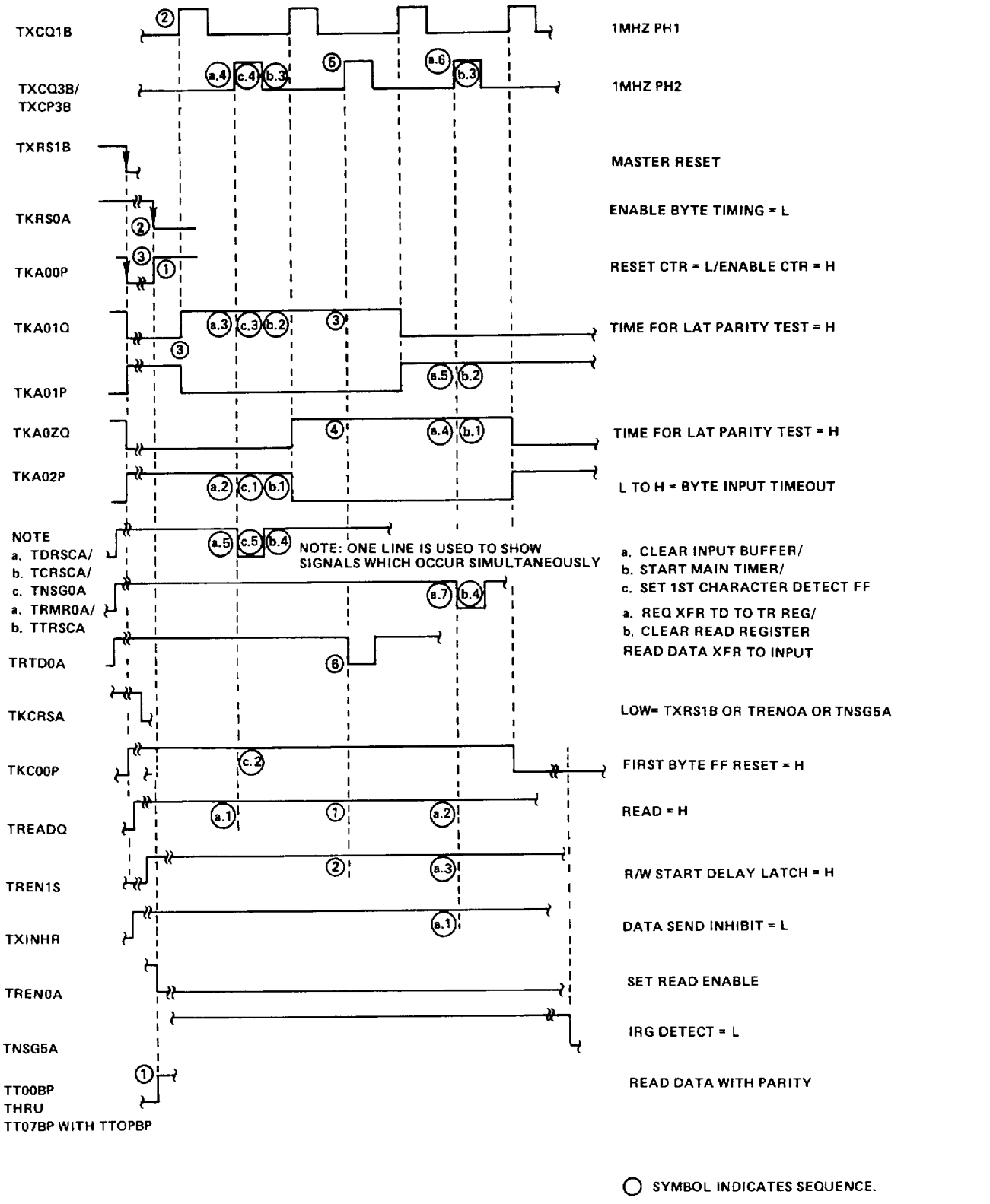


Figure 5-38. Read Byte Counter Timing Diagram

pulse and internal signal TKA02P as it makes a low to high transition on the fourth TXCQ1B clock pulse.

b. First Byte Flip-Flop (FF) (fig. 5-37 and 5-38). The first byte, is significant for the timing of the interrecord gap detect logic. Initially, the master reset signal (TXRS1B) resets the first byte I/O timeout = L/first byte FF reset = H signal (TKCO0P) to high. The low set read enable signal (TREN0A) resets the flip-flop when a read or write command is received. The low to high transition of internal signal TKA02P clocks out the low TKC00P from the flip-flop. Signal TKC00P remains low until a new command or an interrecord gap (IRG) is detected. Therefore, the high TKC00P effectively represents the first byte. The IRG detect = L signal (TNSG5A) resets the flip-flop after the IRG detects a 20-ms delay in which no byte of read data occurs.

c. Timing Decoder (fig. 5-37 and 5-38). The decoder receives the counter outputs and control signal inputs from other functions and when the necessary inputs are coincident, the phase two clock produces the corresponding output signals. Table 5-3 shows the input/output relationships.

5-23. Record Gap Detect Logic (fig. 5-39). The record gap detect logic is located in the card cage. The function of this logic is to detect the interrecord gap (IRG) on the magnetic tape. The gap contains no data. The gap is detected for high and low speeds. The logic also functions to detect erroneous conditions of no data. The logic is subdivided into the following blocks.

Low speed gap detect
Interrupt decoder
High speed gap detect

These blocks are explained in the following subparagraphs.

a. Low Speed Gap Detect (fig. 5-39 and 5-40). The main timing counter is started by the first byte of data read from the tape for either the read or write function. At the same time, the gap detect logic is set. The main timing counter is restarted for every byte of data read from the tape. If no byte is read, the counter continues counting out to 75 µs. At this

Table 5-3. Timing Decoder Truth Table

	READ ONLY	BOTH R&W	BOTH R&W	READ ONLY	BOTH R&W	READ ONLY
INPUT						
TKAO1Q	1	1	1	0	X	1
TKAO1P	0	0	X	1	1	X
TKAO2Q	0	0	X	1	1	1
TKAO2P	1	1	1	0	X	X
TKCOOP	X	X	1	X	X	X
TREADQ	1	X	X	1	X	1
TREN1S	X	X	X	1	X	1
TXINHR	X	X	X	I	X	X
TXCQ3B OR TXCP3B	1	1	1	1	1	1
OUTPUT						
TDRSCA	1					
TCRSCA	1					
TN5GOA		1				
TRMROA			1	1		
TTRSCA				1	1	
TRTDOA						1

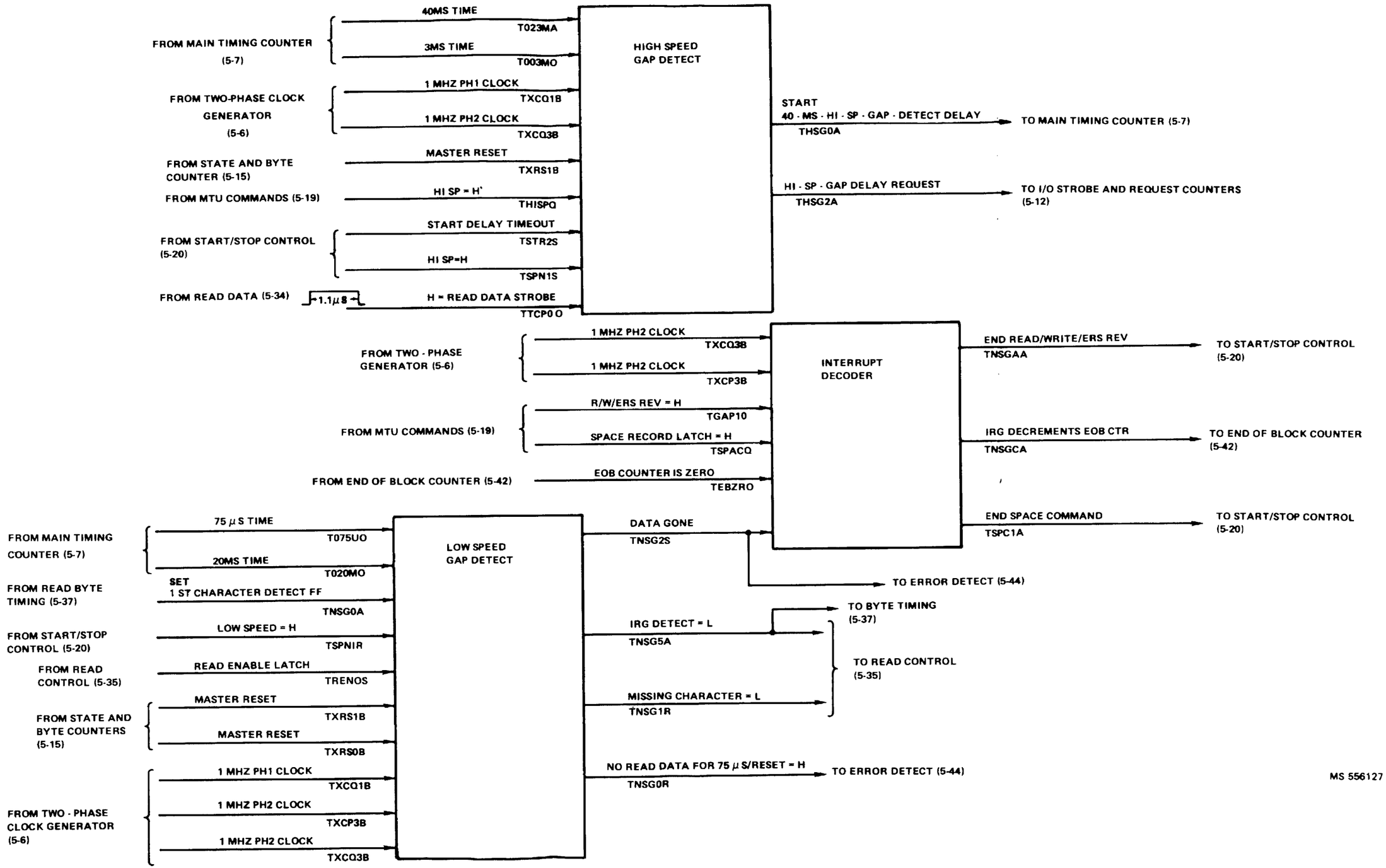


Figure 5-39. Record Gap Detect Block Diagram

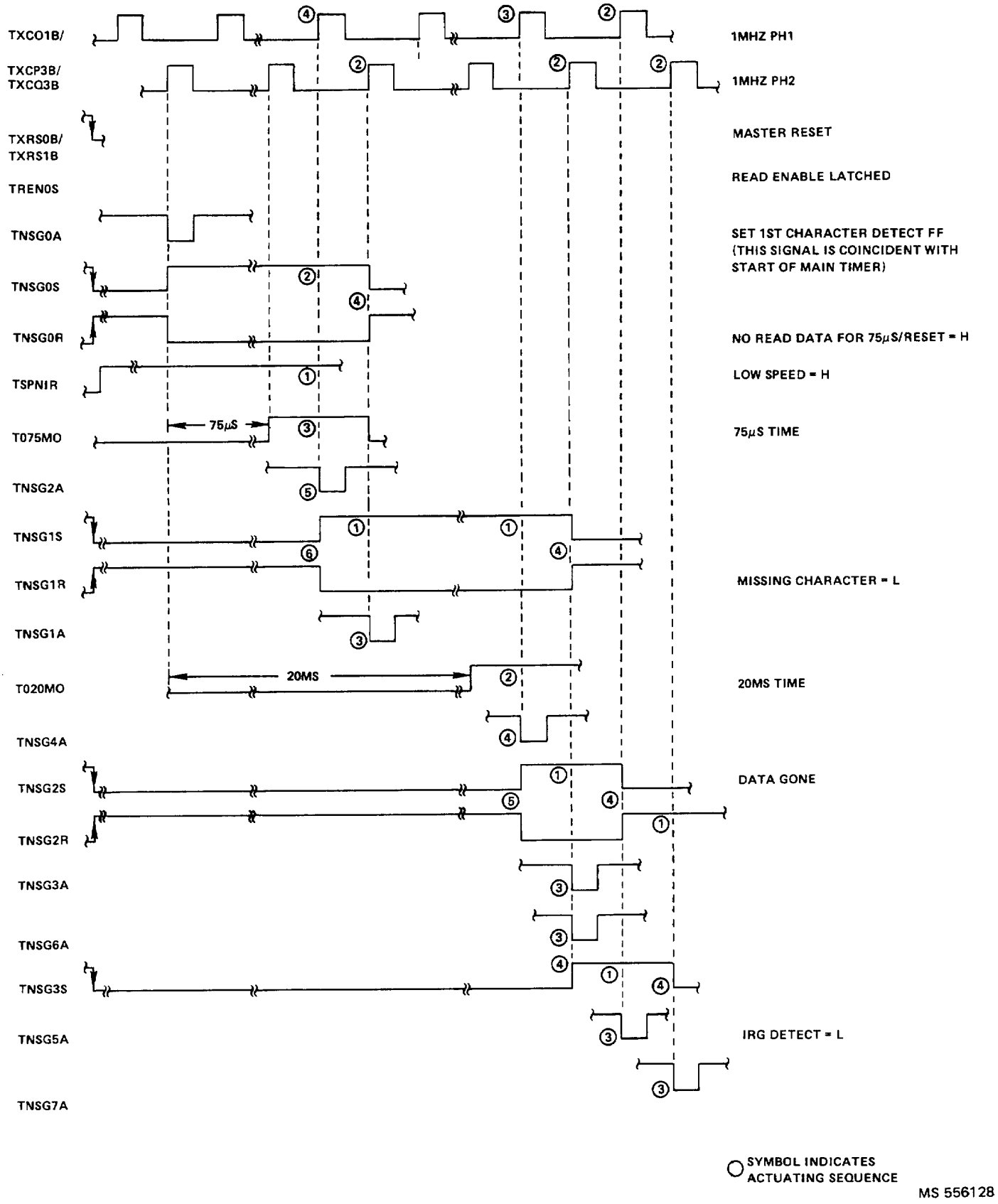


Figure 5-40. Record Gap Detect Timing Diagram

time an input to the gap detect logic indicates one character is missing. If the counter continues until the 20-ms time is detected, an IRG is indicated. The master reset signals (TXRSOB and TXRS1B) reset internal signals TNSGOS, TNSG1S, and TNSG3S to low; the data gone signal (TNSG2S) to low; and the no read data for 75 µs/reset = H signal (TNSGOR) to high. The set 1st character detect-FF signal (TNSGOA), which is coincident with the start of the main timer, sets TNSGOS to high and TNSGOR to low. With the low speed =H signal (TSPNIR) at a high level and TNSGOS high, the next 1-MHz PH1 clock (TXCQIB) produces TNSG2A. Signal TNSG2A goes low and sets TNSGIS to high and TNSG1R to low. With TNSG1S high, the next I-MHz PH2 clock (TXCP3B) produces the low TNSG1S that resets TNSGOR to high and TNSGOS to low. With TNSG1S high, when the 20-ms time signal (T020MO) goes high indicating an (IRG), the next TXCQ1B clock pulse produces internal signal TNSG4A, TNSG IS that resets TNSGOR to high and TNSGOS to low. With TNSG S which sets TNSG2S to high and its complement TNSG2R to low. With TNSG2S high, the next phase two clock produces the internal signals TNSG3A and TNSG6A. Signal TNSG6A sets TNSG3S to high. With TNSG3S high, the next TXCQIB produces the IRG detect signal (TNSG5A). The low TNSG5A resets TNSG2S to low. This completes the cycle for one IRG. If the MTU is commanded by the ADP to space, the cycles continue and TNSG2S is generated for each IRG.

b. Interrupt Decoder (fig. 5-39). For the read, write, or erase reverse functions, when an IRG is detected, the decoder provides an end read/write/erase reverse (ERS REV) signal (TNSGAA). If the space function is in operation, each data gone signal (TNSG2S) produces the IRG decrements end of block counter (EOB CTR) signal (TNSGCA). While still in the space function, and the EOB is zero, TNSG2S produces the end space command signal (TSPC1A). Table 5-4 is the truth table for the three outputs of the decoder. The table shows the required inputs including the clocks for each output.

Table 5-4. IRG Interrupt Decoder Truth Table

INPUTS			
TXCQ3B	1	X	X
TXCP3B	X	1	1
TGAPIO	1	X	1
TSPACQ	X	1	1
TEBZRO	X	X	1
TNSG2S	1	1	1
OUTPUTS			
TNSGAA	1	X	X
TNSGCA	X	1	1
TSPCIA	X	X	1

c. High Speed Gap Detect (fig. 5-39 and 5-41). This logic receives the read data strobe and produces a signal that starts the main timing counter. As long as data is read, the main timing counter restarts for each read data strobe. When the IRG on the tape is reached, no data is read, so the counter continues running and produces the 3-ms time signal for the high speed detect, which then produces a request to the ADP. The ADP counts the requests in the alarm mode and issues an EOB command when the block length field of its I/O keyword is decremented to zero. Initially, the high speed gap detect is reset by the mater reset signal (TXRS1B). The low TXRS1B resets internal signals THSGOS and THSGIS to low and THSG1R to high. With the high speed (HI SP)= H signals (THISPQ and TSPNIS) set high, and the start delay timeout signal (TSTR2S) set high, when the H = read data strobe signal (TTCPOO) goes high, the next 1-MHz PH2 clock (TXCQ3B) produces the output signal start 40ms HI SP gap detect delay (THSGOA). The low THSGOA also sets internal signal THSGOS to high. With THSGOS high and the 3-ms time signal (T003MO) high (indicating an IRG), the next 1-MHz PHI clock (TXCQIB) produces the output signal HI SP gap delay request (THSG2A). The low THSG2A also sets THSG IS to high and THSG1R to low. With THSG1S high, the next TXCQ3B produces the low THSGIA that resets THSGOS to low. The main counter is not restarted and at 40 ms, the 40-ms time signal (T023MA) goes low. This resets THSG1S to low and THSG1R to high and enables the input for another cycle. The cycles continue generating a request to reach IRG until the block-length field of the I/O key word in the ADP's IOU is zero. The zero initiates an end of block (EOB) command to the MTU from the ADP for the alarm mode (a mode in which events such as data records are counted). No data is transferred in the alarm mode.

5-24. End of Block (EOB) Counter (fig. 5-42).
The EOB counter logic is located in the card cage. This logic functions as a preset counter that is decremented by clocks created by either end-of-block commands in read or write operations or by the interrecord gap (IRG)

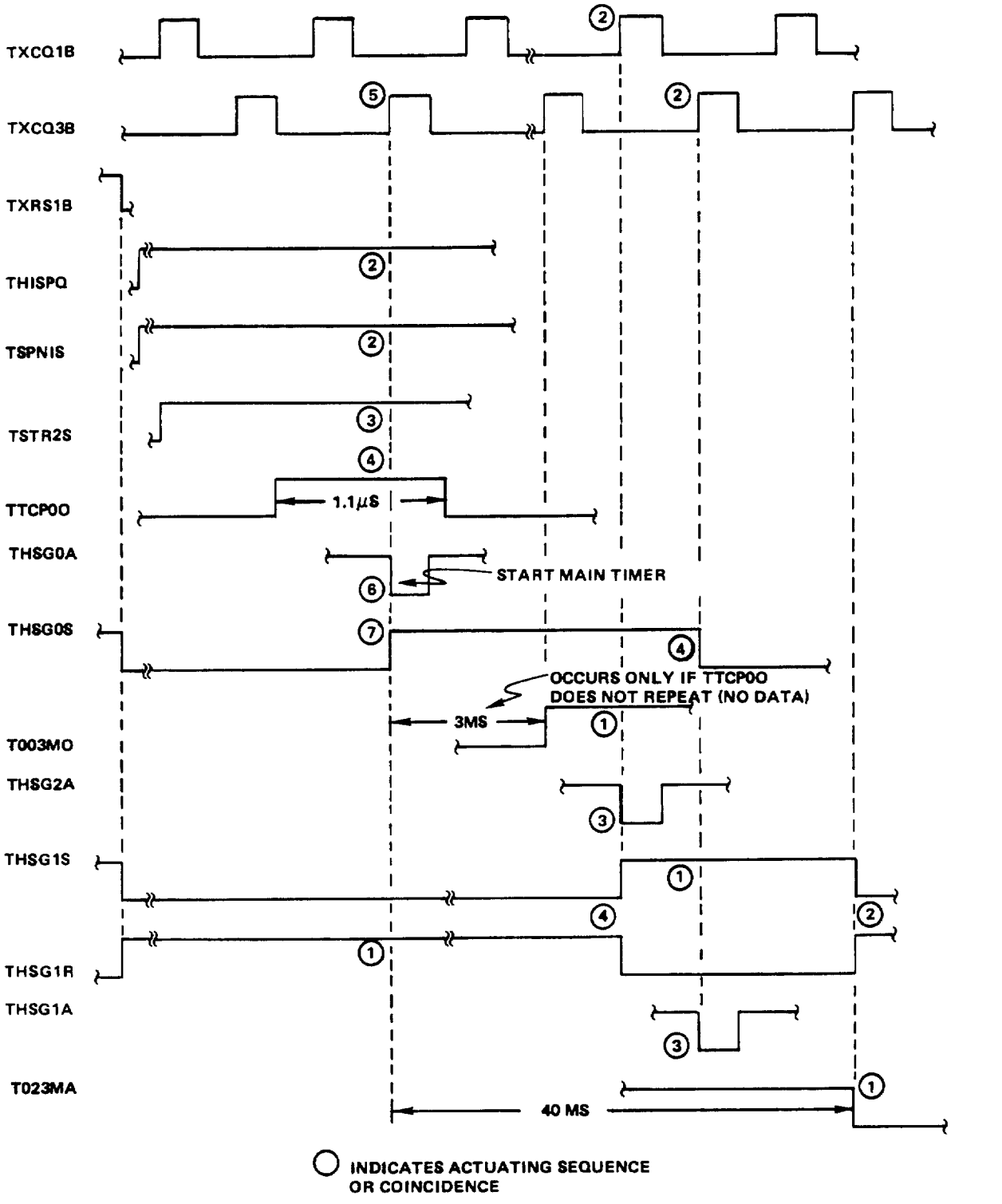


Figure 5-41. High Speed Gap Detecting Timing Diagram

in the space operation. The logic is subdivided into the following functions.

Preset count gate
EOB clock generator
EOB counter
Zero count decoder

a. Preset Count Gate. The first 4 bits of the third byte of the command phase contain the preset count code. These 4 bits are the preset count signals (TXSOBQ through TXS3BQ). In the example operation shown by the timing diagram (see figure 5-43), the binary code is 1111, representing a block count of 15. A code of 1111 means that TXSOBQ through TXS3BQ are all at a high logic level. The high device command (DEVCMD) clock signal (TXDV1B) produces the low clocked preset count signals (TEBSOA through TEBS3A).

b. EOB Clock Generator. When the zero count= clock disable signal (TEBZRA) is high, the clock can be generated either by the EOB command when enabled by either read or write commands, or by the IRG in space forward or reverse operation. Either the read =L signal (TREADP) or the write = L signal (TWRITP), when low, produces the high output signal read or write command (CMD) (TRWC10). Also, with TRWC10 high, when the SYNCED EOB CMD signal (TXEBIQ) goes high, the next I-MHz PH2 clock (TXCP3B) generates the EOB clock (TEBCPA). The clock is a negative pulse with a 62.5pus width. The counter is clocked by the positive going trailing edge. With TEBZRA high, TEBCPA is also generated when the IRG decrements EOB counter (CTR) signal (TNSGCA) goes low. When TEBZRA goes low at reset or at zero count, the clock is forced high, effectively disabling the clock.

c. EOB Counter. The counter is reset during the second byte of the command phase by the reset EOB counter signal (TEBRSA). When TEBRSA goes low, all of the all high = zero count signals (TEBOBP through TEB3BP) go high. During the third byte of the command phase, the clocked preset count signals (TEBOSA through TEB3SA) set the flip-flops of the counter to the designated count. In the example of figure 5-43, all flip-flops are set. Therefore, all TEBOBP through TEB3BP outputs go low. At the end of the third byte of the command phase, the signal end of 3rd CMD byte =H (TXDEVR) goes high, enabling the data inputs of the first three flip-flops. This allows the counter to count down when clocked. When the positive-going trailing edge of the clock occurs, the least significant bit (LSB) flip- flop changes state. The count is shown in figure 543. When internal signals TEBOBP through TEB3BP are all high, the countdown equals zero, and thereby signals the completion of the current command.

d. Zero Count Decoder. When internal signals TEBOBP through TEB3BP all go high, either by reset or by the zero count, zero count = clock disable signal TEBZRA goes low, disabling the EOB clock. Also, when TEBZRA goes low, it is inverted to produce the high zero count signal (TEBZRO).

5-25. Error Detect Logic (fig. 5-44 and 5-45). The error detect logic is located in the card cage with the exception of the power supply fault function that includes the FAULT RESET switch-indicator on the front panel. The logic tests the read and write magnetic tape data and the lateral parity of the data as it arrives from the ADP. It also tests the data on the magnetic tape during write or read commands for longitudinal parity. Other errors detected in the MTU are accepted by the logic. Each of the errors latches the FAULT RESET switch-indicator. The FAULT RESET switch indicator is pressed momentarily to reset the latch. The logic is subdivided into the following functions.

Longitudinal redundancy check (LRC) register
Longitudinal parity error detector
Read/write register parity checker
Lateral parity error detector
I/O register (input) parity checker
Write data parity error detector
No-data error detector
Timing error detector
Error register
Parity error detector
Fault reset logic
Error register reset logic

a. Longitudinal Redundancy Check (LRC) (fig. 545). This is a test to determine if all of the bits that are supposed to be written can be read. The lateral parity error checker performs the same function but in a different way. Therefore this test is redundant. However, if only one of the tests was used, if an even number of bits in a byte were not read or an even number of bytes had the same bit missing,

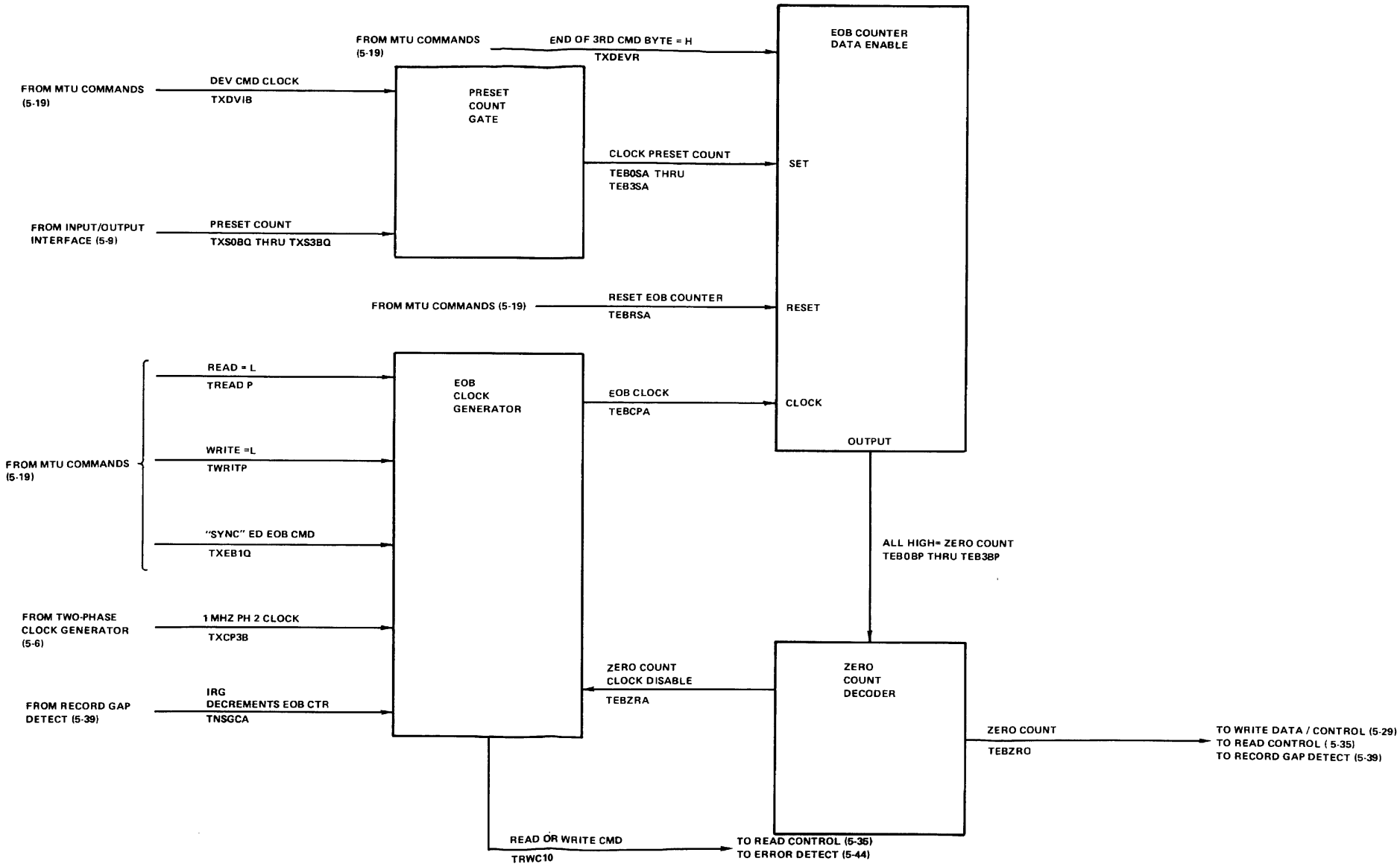
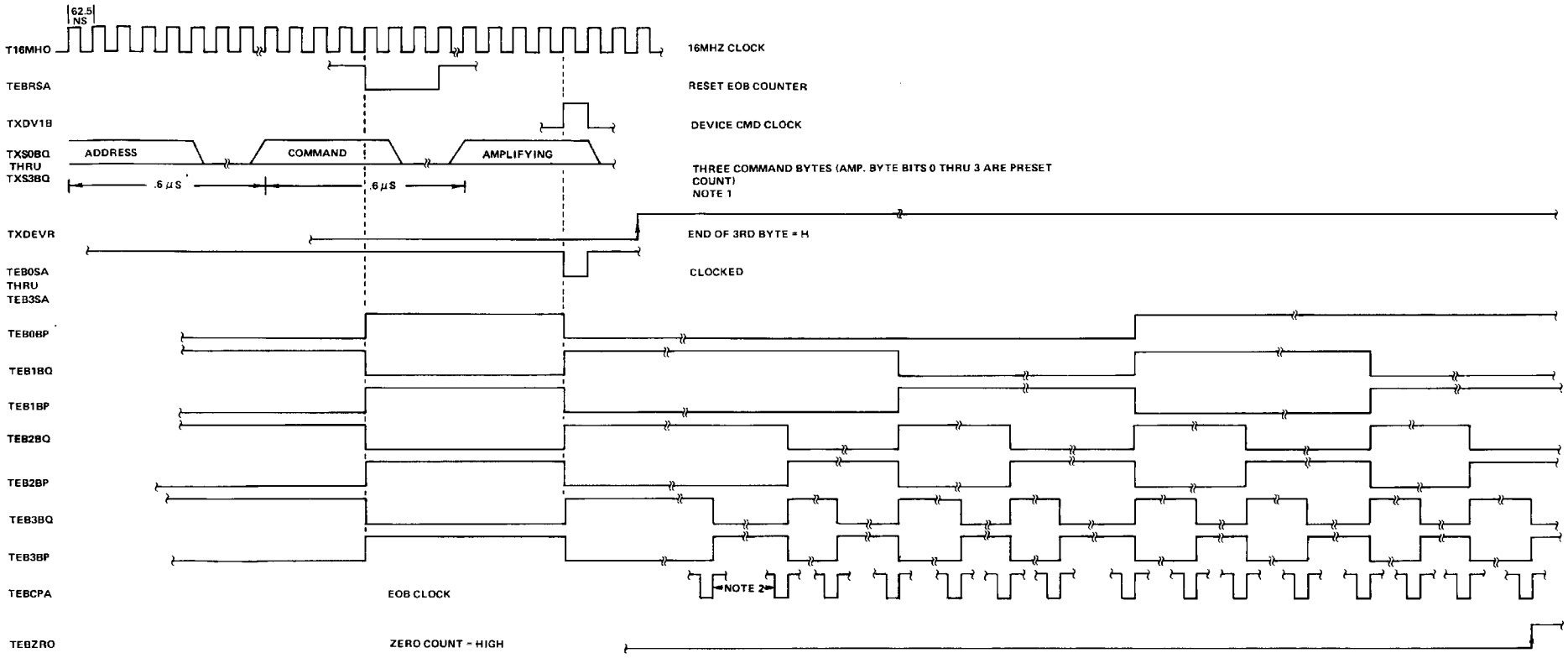


Figure 5-42. End of Block Counter Block Diagram



NOTES:
1. PRESET COUNT ASSUMED TO BE 15 = BINARY 1111 FOR THIS DIAGRAM
2. DATA RECORD LENGTH MAY VARY UP TO A MAX OF 8192 32-BIT WORDS = 32768 BYTES, WHICH EQUALS 16 BLOCKS OF 2048 BYTES EACH. 15 OR LESS EOBS DECREMENT THE COUNTER. THE 16TH OR NEXT EOB CAUSES READ OR WRITE TO STOP.

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Figure 5-43. End of Block Counter Timing Diagram

no error would be detected. Using both tests, any failure to read a bit that has been written will result in an error. The test uses the LRC counter and the LRC register in addition to the write and read logic (see figure 5-45). The P outputs of the write JK flip-flops are reset to high by the write syncronizer counter or the MTT control logic (see the RESET sequence in figure 5-45). When the first byte of the write data is clocked in, each high level bit to both the J and K inputs causes the P output to go low and the Q output to go high. With + 5v from the MTT control logic applied, switching the low side of the record head causes current to flow, generating a flux change on the tape. This is a nonreturn-to-zero method of recording. The flux change is immediately picked up by the reproduce head, creating a read bit voltage waveform that is shaped and deskewed. The read bit also creates the node output to the MTT control logic. The MTT control logic responds with a clock that transfers the data to the read data logic. After a short delay, the MTT control logic sends a strobe to transfer the read data to the LRC register. If a read data bit is high, it clocks one of the LRC register flip-flops. The Q output toggles from high to low or low to high each time it is clocked. The second write data byte is applied to the JK flip-flops and each bit that is a 1 causes the levels of the JK flip-flop outputs to toggle. The new output levels cause a change in magnetic flux on the tape by the record head. The flux change is detected by the reproduce head and converted to a read bit by the read amplifier. The read data is clocked to the LRC register where each high read data bit clocks the corresponding flip-flop of the LRC register. The LRC counter produces a 390µs delay at the completion of the write data. At the end of the delay, the LRC counter produces a signal that resets all of the JK flip-flop P outputs to high if they are not already high. For each output that is toggled to a high level, a bit is recorded, reproduced, and transferred to the LRC register. Each JK flip-flop that has a Q output at a low level must receive a clock at this time if there is no error. The high read data bits clock the LRC flip-flop outputs to high. At a time determined by the conditional logic, the high LRC outputs produce a no-error signal. If any one of the LRC outputs are low at this time, and only at this time, an error signal is produced. The input and output signals of the LRC register and longitudinal parity error detector are discussed in the following subparagraphs.

(1) *LRC register (fig. 5-44).* Initially, the LRC register *low when data gone = error* output signals (TLRCOQ through TLRC7Q and TLRCPQ) are set high when the *read or write command CMD* signal (TRWC10) and the *volts to write head* signal (TSNC1S) are both high and the *1 - MHz PHI* clock (TXCQ1B) goes high. The *read data with parity = H* signals (TTOOBQ through TT07BQ with TTOPBQ) when high, clock the TLRCOQ through TLRC7Q and TLRCPQ output signals. Each clock toggles the corresponding output from high to low and as the bytes of 9-bit read data continue to clock the LRC flip-flops, the outputs continue to toggle low to high and high to low.

(2) *Longitudinal parity error detector (fig. 544). The low when data gone = error* signals are applied to the detector. When TRWC10 and TNSG2S are high, the next TXCQ3B produces a low TLNGSA if any one of TLRCOQ through TLRC7Q and TLRCPQ are low.

b. Read Register Parity Checker (fig. 5-44). For the 9-bit word composed of 8 bits of data and 1 bit for parity, there is always an odd number of bits. If the 9-bit word contains an even number of bits, an error is indicated. *The read data with parity = L/ reset = L* signals (TTOOBP through TT07BP with TTOPBP) and the *read data with parity* signals (TTOOBQ through TT07BQ with TTOPBQ) are sent to the read register parity checker. The simplified truth table for this block always shows a low output when the number of high Q inputs is odd. If the number of high Q inputs is even (error condition), the *high when checked = error* output signal (TRPCEO) is high.

NO. OF HIGH INPUTS	OUTPUT
1 = ODD 0 = EVEN	0 = LOW 1 = HIGH
1 0	0 1

c. Lateral Parity Error Detector (fig. 5-44). The high when checked = error signal (TRPCEO) input to the detector is a result of the latched read data inputs. Therefore, it maintains its logic level until the time determined by the conditional logic. When the read or write command CMD signal (TRWC 10) and the *read/write (R/W) start delay latch = H* signal

(TREN1S) are both high and TRPCEO goes high, the next 1-MHz PH2 clock (TXCP3B) goes high and allows the combination of the high time for lateral parity = H signals (TKA01Q and TKA02Q) to clock out the active low *set lateral parity = L* signal (TLATSA).

d. I/O Register (Input) Parity Checker/Read, Status, or Interrupt Parity Bit Generator (fig. 5-44). The parity check functions to test the data to the MTU from the ADP. This consists of either commands, write, or loop test data. The test determines if there is a parity bit when the number of data bits is even, or that there is no parity bit when the number of data bits is odd. The parity bit generator functions to generate a parity bit when necessary for either the read, status, or interrupt output data when the MTU is not in write or loop test.

(1) *I/O register (input) parity checker (fig. 544).* The *input data signals* (TXSOBQ through TXS7BQ) from the I/O register of the I/O interface are active high. The *input data** signals (TXSOBP through TXS7BP) are the inverse of the Q input signals: The *parity bit* signal (TXSPBQ) is also active high with *parity** (TXSPBP) the inverse.

(a) Intermediate outputs. Refer to table 5-5 for the I/O parity truth table. When the number of high Q input signals are odd, and the parity bit is high, both the output signals *no parity bit/error = L* (TPD60A) and *parity bit/error = L* (TPD6 1A) are high. When the number of high Q input bits is even and the *parity bit** (TXSPBP) is high, outputs TPD60A and TPD61A are also high for this logic. The error conditions are as follows:

1. With an odd number of high Q input data signals and the *parity bit* (TXSPBQ). high, TPD61A goes low.
2. With an even number of high Q input data signals and the *parity bit** (TXSPBP) is high, TPD60A goes low.

(b) Final Outputs. Refer to table 5-5 for the I/O parity truth table. With TPD60A, TPD61A, and the *computer data error = L* signal (TCDERP) all high, there is no error indicated. When either TPD60A or TPD61A goes low, the computer data error signal (TCDERO) and the write data parity error signal (TXROPO) go high. The computer data error = L signal (TCDERP) is a feedback signal that latches TCDERO high.

(2) *Read, status, or interrupt parity bit generator (fig. 5-44).* When the number of high Q input data signals is odd and the device or loop test* signal (TXXCIP) is high (low = write or loop test), odd = L/even = H output parity check output signal (TPS60A) is low (refer to table 5-5). If the number of high Q input data signals is even, TPS60A is high when TXXCIP is high.

e. Write Data Parity Error Detector (fig. 5-44). Each new byte of input data is checked. When the enable is latched signal (TXENAS) is set high and then when the new byte of input data results in the write data parity error signal (TXROPO), the logical combination of the high state count 5 (TXXAOP) and state count 2 (TXXA1Q) signals causes a check of the byte in the I/O register. If the byte is in error (indicated by a high TXROPO), the write CMD data parity error (TXDPEA) signal goes low.

f. No-Data Error Detector (fig. 5-44). The no data error detector logic produces the error indication set no data error flip-flop (FF) signal (TNDTSA). Signal TNDTSA is low when clocked by the 1-MHz PH2 clock (TXCP3B) and the following logic is satisfied: 1-MHz PH2 clock (TXCP3B) is active high, rewind latch = L (TREWDP) is high, no erase FWD = H (TERSFP) is active high, and any one of the following combinations is present:

65 ms sets latch = H (TWRIOS) is active high
AND
no read data for 75 µs = H (TNSGOR) is high = error
AND
150-ms time (T150MO) is active high OR
start delay timeout (TSTR2S) is active high AND
same speed = H (TSPNSP) is active high AND
1.8-sec timeout (TSTR2S) is active high OR
on-line (TONLNS) is active high AND
new speed = H (TSPNSQ) is high AND
1.0-sec time (TC60BP) is active high

g. Timing Error Detector (fig. 5-44). The timing error detector logic simply provides a logical OR function. Either the active low read timing error signal (TRTOCA) or the active low data not ready = timing error = L signal (TWTOCA) produces the active low read or write timing error signal (TTMESA).

h. Types of Errors and Fault Reset (fig. 5-44). This logic consists of the error register, fault reset logic, parity error detector, and error register reset logic functions. The errors set the flip-flops of the error register. The detached high Q outputs of the error register flip-flops make up part of the status

Table 5-5. I/O Parity Truth Table

a. Intermediate Outputs

INPUTS				OUTPUTS				
ODD NO. Q = H INPUTS	EVEN NO. Q = H INPUTS	PARITY Q = H	PARITY P = H	TXXCIP	TPD60A	TPD61A	TPS60A	
1	0	0	1	0	1	1	0	WRITE OR LOOP TEST
0	1	1	0	0	1	1	0	NO ERROR CONDITION
1	0	X	X	1	X	X	0	READ, STATUS,
0	1	X	X	1	X	X	1	OR INTER-RUPT PAR-ITY BIT GENERATOR
1	0	1	0	0	1	0	0	WRITE OR LOOP TEST
0	1	0	1	0	0	1	0	ERROR CON-DITIONS

b. Final Outputs

LOGIC		ERRORS		
TPD60A	TPDG1A	TCDERP	TCDERO	TXROPO
1	1	1	0	0
1	1	0	1	0
1	0	X	1	1
0	1	X	1	1

0 = LOW

1 = HIGH

ODD NO. OF Q = H INPUTS:

1 = TRUE, 0 = FALSE

EVEN NO. OF Q = H INPUTS:

1 = TRUE, 0 = FALSE

X = IRRELEVANT

or interrupt bytes which are sent to the ADP through the read, status, or interrupt output and the I/O interface. The corresponding latched low P outputs of the error register are applied to the fault reset logic, causing the FAULT RESET switch-indicator to light. The power supply also provides a fault signal which can light the indicator. To reset the error register, the FAULT RESET switch-indicator is pressed momentarily. The switch output goes to the error register reset logic, the output of which resets the error register. The P outputs go high, and the FAULT RESET indicator goes off.

(1) *Error register*. There are six error flip-flops as follows: Lateral parity error, no-data error, longitudinal parity error, read or write timing error, file protect error, and computer data error.

(a) Set the error flip-flop. The low inputs set the flip-flop Q outputs high and the P outputs low (refer to table 5-6).

(b) Clock the error flip-flop. The high computer data-error signal (TCDERO) is clocked through the flip-flop by the active input register clock (TDCP10O), thereby producing the high computer data parity error (TCDERQ) and computer data error L (TCDERP) signals.

(2) *Fault reset logic.* The momentary low lamp test signal (TLMPTA1), any one of the latched low P output signals (refer to table 5-6), or the fault signal from the power supply provides a low to the ground side of the lamp used to light the FAULT RESET switch-indicator. Power in the form of + 5v, is applied to the other side to light the indicator. When the fault is from the error register, resetting the register removes the power ground and the indicator goes off. One way the register is reset is by manually pressing the momentary FAULT RESET switch-indicator. This provides the active low switch resets register signal (TERSTR) to the error register reset logic.

(3) *Error resistor reset logic.* The master reset (TXRSQB), new CMD resets error register (TSNC2A), OFR set (TXODRA), or switch resets register (TERSTR) signals, when low, produces the low error register reset signal (TERROA). Signal TERROA resets each of the six flip-flops in the. register.

(4) *Parity error detector.* Either the lateral parity error = L signal (TLATEP) or the longitudinal parity error = L signal (TLNGEP), when. low, produces the high LAT/LONG parity error signal (TTPERO).

5-26. Beginning of Tape/End of Tape (BOT/EOT) Detect Logic (fig. 5-46). The BOT/EOT detect logic is located in the card cage except for the BOT/EOT indicators on the front panel. The purpose of this logic is to synchronize to the MTU clock the stop sequence initiated by either the BOT detection in reverse or the EOT detection in forward operation. Its purpose is also to light the BOT/EOT indicator on the front panel when a stop sequence is initiated. The logic consists of the BOT/EOT SYNC counters and the BOT/EOT indicators.

a. BOT/EOT SYNC Counters (fig. 5-46 and 5-47). The two counters are identical; therefore, only the BOT SYNC counter is described. To understand EOT operation, substitute EOT for BOT for all the following signal names. The sequence is initiated when the MTT begin of tape signal (XBOTIA) or the MTT end of tape signal (XEOT1A) goes low. When XBOT1A goes low, the BOT received (RCVD) signal (TBOTCO) goes high (see figure 5-47). The next 1-MHZ PH2 (TXCP3B) clock pulse produces the active low internal signal TBOTOA which sets the begin of tape signal (TBOTOS) to high and the begin of tape = L signal (TBOTOR) to low. With internal signal TBOT2R high, when TBOTOS goes high, the next I-MHZ PHI clock (TXCQ1B) produces the active low internal signal TBOT2A which sets the BOT counter (CTR) bit I signal (TBOT1S) to high, and internal signal TBOTIR to low. The high TBOT1S signal goes to the start/stop control where it initiates an interrupt if the MTT is in reverse (forward EOT). The interrupt starts the MTT stop sequence and causes the MTT stop in progress = L signal (TSTPOR) to go low. The low TSTPOR (indicated by dashed lines in figure 5-47) prevents the TBOTOS signal from being reset low. The TBOTOS signal to the indicator remains high. If the MTT is in forward operation (reverse for EOT) TSTPOR stays high. With TSTPOR high, when the tape moves away from BOT, XBOT1A goes high. The BOT SYNC counter continues to count; and while TBOT1S is high, the next TXCP3B clock pulse produces the active low internal signal TBOT4A that sets TBOT2S high and TBOT2R low. With TBOT2S high, the next TXCPLB clock pulse produces the active low TBOT3A which resets TBOTIR high and TBOTIS low. With TSTPOR, and XBOTIA high, when TBOTIR goes high the next TXCQ3B clock pulse produces the active low signal TBOTIA. Signal TBOTIA resets TBOTIS low and TBOTOR high. Signal TBOTOS is energized for only 2gts. The low TBOTOS latches TBOTIS low and TBOTIR high, and resets TBOT2S low and TBOT2R high in preparation for receipt of another low XBOTIA.

Table 5-6. Set Error Register Inputs and Outputs

INPUTS	OUTPUTS
set lateral parity = L (TLATSA)	lateral parity error (TLATEQ)
set longitudinal = L (TLNGSA)	lateral parity (LAT PAR) error = L (TLATEP)
set file protect error (TFPE1A)	longitudinal parity error (TLNGEQ)
set no data error flip-flop (FF) (TNDTSA)	longitudinal parity (LONG PAR) error = L (TLNGEP)
read or write timing error (TTMESA)	file protect error (TFPERQ)
	file protect error = L, (TFPERP)
	no data error (TNDATQ)
	no data error = L (TNDATP)
	read/write (R/W) I/O timing error (TTMERQ)

b. BOTIEOT Indicators (fig. 5-46). When either the begin of tape signal (TBOTOS) or the end of tape signal (TEOTOS) goes high either the BOT or the EOT indicator is lighted. When the lamp test = H signal (TLMPTO) goes high, both indicators light.

5-27. Test Command Generator (fig. 5-48 and 549). The test command generator logic is located in the card cage with the exception of the switches and indicators on the front panel. When the MTT is off-line from the ADP, this logic has the function of producing a 3-phase command sequence that simulates the 3-phase command sequence from the ADP for the operations selectable on the front panel. These are REWIND, FORWARD, and TEST. When FORWARD is selected, the third byte amplifying command is high-speed forward. When TEST is selected, the third byte amplifying command is read. When REWIND, is selected the third byte code results in reverse speed. The logic generates the timing of the three bytes of the command phase, coded address, and device command and for the first and second bytes, respectively, for each of the third byte amplifying commands. For the rewind and forward operations, this logic is reset at the completion of the third byte of the command phase. For forward operation, the tape continues to run to the end of tape (EOT) in the forward direction because the requests generated by the I/O strobe and request counter are inhibited. The inhibit is initiated by the output of the record gap detector for high speed operation. When ON-LINE is selected, the requests generated by interrecord gaps are sent through the I/O interface to the ADP where an end of byte command (EOB CMD) is generated. The EOB CMD is sent to the MTU through the I/O interface and MTU commands logic. For high speed operation this causes an interrupt in the start/stop control and initiates the stop sequence. For rewind operation the tape runs at normal speed to the beginning of tape (BOT) in the reverse direction. The BOT or EOT is deleted by the BOT/EOT detect function. This function provides an output to the start/stop control, and the start/stop control generates an interrupt that initiates the stop sequence. For test operation, the test command is active until as a result of the first IRG the record gap detector sends an output to the start/stop control. The start/stop control generates an interrupt that initiates the stop sequence. At the completion of the stop delay, a signal is sent by the start/stop control to the test command generator to reset the test command. The test command generator logic is subdivided into the following functions.

Front panel switches
Rewind and forward latches
Test and on-line latches
Front panel indicators
Reset logic
Generated byte counter
State clock enable
Generated state counter Generated byte encoder

a. Front Panel Switches (fig. 5-48). The REWIND, FORWARD, and TEST switches in a normal position provide, respectively, the normal = L signals (TMRWNO4, TMFWDO4, and TMTSTO4). The switches are spring loaded in the normal positions. When actuated, they provide the corresponding output signals rewind = momentary low (ML) (TMRWNA4), forward = ML (TMFWDA4), and test = ML (TMTSTA4). The ON-LINE switch is actuated to provide the on-line = low signal (TONLNA4). When the switch is not actuated, the off-line = low signal (TONLNO4) is active.

b. Rewind and Forward Latches (fig. 5-48). When the rewind = momentary low (ML) signal (TMRWNA4) goes low, the output signal, rewind reset (RST) = momentary low/counter flip-flop (MLI CTR F) enable = H (TMRWNR) is latched low. When TMRWNO4 goes low, TMRWNR is latched high. When TMRWNR goes low, the command (CMD) is rewind output signal (TMRWSS) is latched high.

(1) *Forward.* When the forward = ML signal (TMFWDA4) goes low, the output signal, CMD is forward (TMFWDR) is latched low. When the TMFWDO4 goes low the output signal TMFWDR is latched high. When TMFWDR goes low, the output signal, TMFWSS is latched high.

(2) *Reset.* When the rewind and forward reset signal (TESTDA) goes low at the completion of the third byte of the command phase, the output signals TMRWSS and TMFWSS are latched low.

c. Test and On-line Latches (fig. 5-48). The test and on-line latches are described in the following subparagraphs:

(1) *Test.* When the test = momentary low (ML) signal (TMTSTA4) goes low, the test reset (RST)ML/ enable = H output signal (TMTSTR) is latched low. When TMSTO4 goes low, TMTSTR is latched high.

(2) *On-line.* When TONLNA4 goes low, TONLNS is latched high and the off-line = H for test signal (TONLNR) is latched low. When TONLNO4 goes low, TONLNS is latched low and TONLNR is latched high. When the MTU is on-line (TONLNS is high) with the ADP, there is two-way communications between the two. When the MTU is off-line (TONLNR is high and TONLNS is low) there is no communication with the ADP. When the MTU is off-line, the logic is affected as follows:

(a) In the read, status, or interrupt output logic, the input enable signal (TXAIEA) is inhibited.

(b) In the I/O interface, the TXAIEA signal-disables the ADP input and enables the test command generator input to the I/O register. The new CMD and MTU enable reset I/O signal (TXARSA) to the I/O strobe and request counters for generating master reset is also inhibited.

(c) In the read control, the read timing error signal (TRTOCA) is inhibited.

(d) In the error detect logic, the no-data error detected after 1 sec signal (TNDA3A) is inhibited (see volume 3, FO-18).

(e) In the write data/control logic, TRWEIO and the data not ready (RDY) = timing erase (ER) = L signal (TWTOCA) are inhibited.

(f) In the address, command, and enable logic, the low TONLNS sets the data send inhibit signal (TXINHR) to low. This prevents the interrupt outputs from being enabled in the read, status, or interrupt output logic. It also disables the request output signal (TXARQA) in the I/O strobe and request counters.

d. *Front Panel Indicators (fig. 5-48).* Front panel indicators are described in the following subparagraphs.

(1) *TEST.* When the test reset (RST) = momentary low (ML) enable = H signal (TMTSTR) goes low, the command (CMD) is test = H output signal (TMTSSS) is latched high. The high TMTSSS produces a low which lights the TEST indicator. When any of the rewind inhibits test (TSTRLA), TXRSOB, or low speed (SP) stop (TSTP8A) signals go low, TMTSSS is latched low and the TEST light goes off.

(2) *READY.* When both the on-line set (TONLNS)and MTT ready to receive (TRDY 1O) signals are high, a low is produced that lights the READY indicator.

(3) *LAMP TEST*. When the LAMP TEST switch is actuated the lamp test signal (TLMPTO) goes high. When TLMPTO is high, it produces a low to the TEST and READY indicators that causes them to light.

e. Reset Logic (fig. 5-48). When any of TMRWNR, TMFWDR, or TMTSTR momentarily go low, the start the state clock signal (TMTR1A) momentarily goes low. When either TMTRIA or TXRSOB is active low, the reset (RST) = L/enable = H signal (TMTROA) is active low.

f. Generated Byte Counter (fig. 5-48 and 5-49). When the signal, TMTRIA goes low, the bytes 1&2 = H signal (TEST6P) is reset high and the byte 3 = H/Low = clock enable signal (TEST6Q) is reset low. Coincident with TMTR1A, the TMTROA signal goes low. Signal TMTROA resets byte I = H/ low = clock enable signal (TEST5P) to high. Signal TEST5P resets the bytes 2&3 = H signal (TEST5Q) to low. When the byte counter clock signal (TEST4P) goes high at the completion of the first byte, the high bytes 1&2 = H signal (TEST6P) is clocked to produce a high bytes 2&3 = H signal (TEST5Q) and a low byte I = H/low = clock enable signal (TEST5P). Signal TEST4P goes high at the end of the second byte and produces the high TEST6Q and the low TEST6P. When TEST4P goes high at the end of the third byte TEST5Q goes low and TEST5P goes high.

g. State Clock Enable (fig. 5-48 and 5-49). When TEST5P and TEST6P go high, the rewind and forward reset signal (TESTDA) goes low. Initially, when TEST6Q goes low during the first byte of the three-byte command sequence, TESTDA goes high. With TESTDA high, the 16-MHz clock signal (T16MIO) produces the state clock-16 MHz signal (TESTKA) which is in effect 180 degrees out of phase with T16MIO.

h. Generated State Counter (fig. 5-48 and 5-49). When the reset (RST) = L/enable = H signal (TMTROA) goes low as a result of selecting either REWIND, FORWARD, or TEST, the TESTOQ, TESTIQ, TEST3Q, and output byte enable I signal (TEST4Q) are reset low and the output byte enable 2 (TEST1P) and the byte counter clock TEST4P signals are reset high. After the momentary low that caused the reset, TMTROA goes high, allowing the next positive-going edge of the state clock = 16 MHz signal (TESTKA) to clock the state counter. The high TEST4P fed back internally to the input, when clocked by the first high TESTKA produces

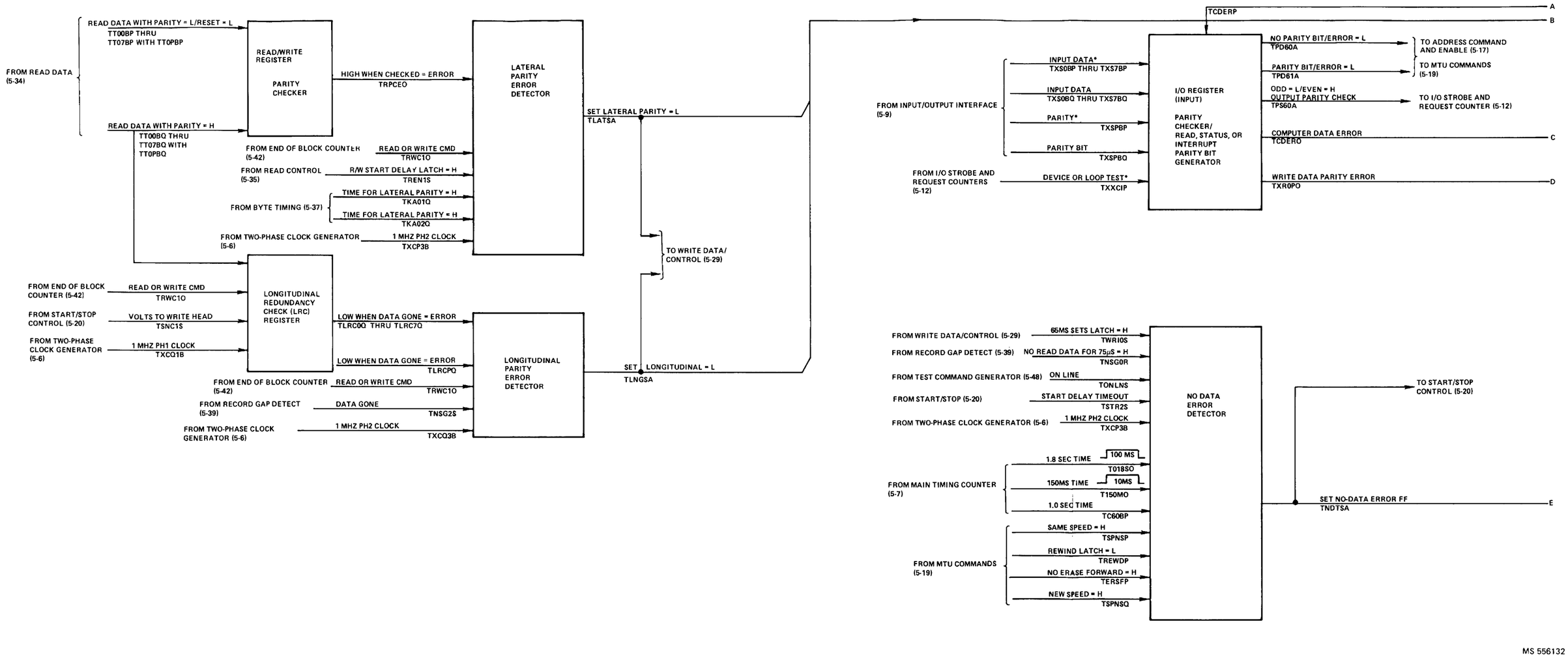


Figure 5-44. Error Detect Block Diagram (Sheet 1 of 2)

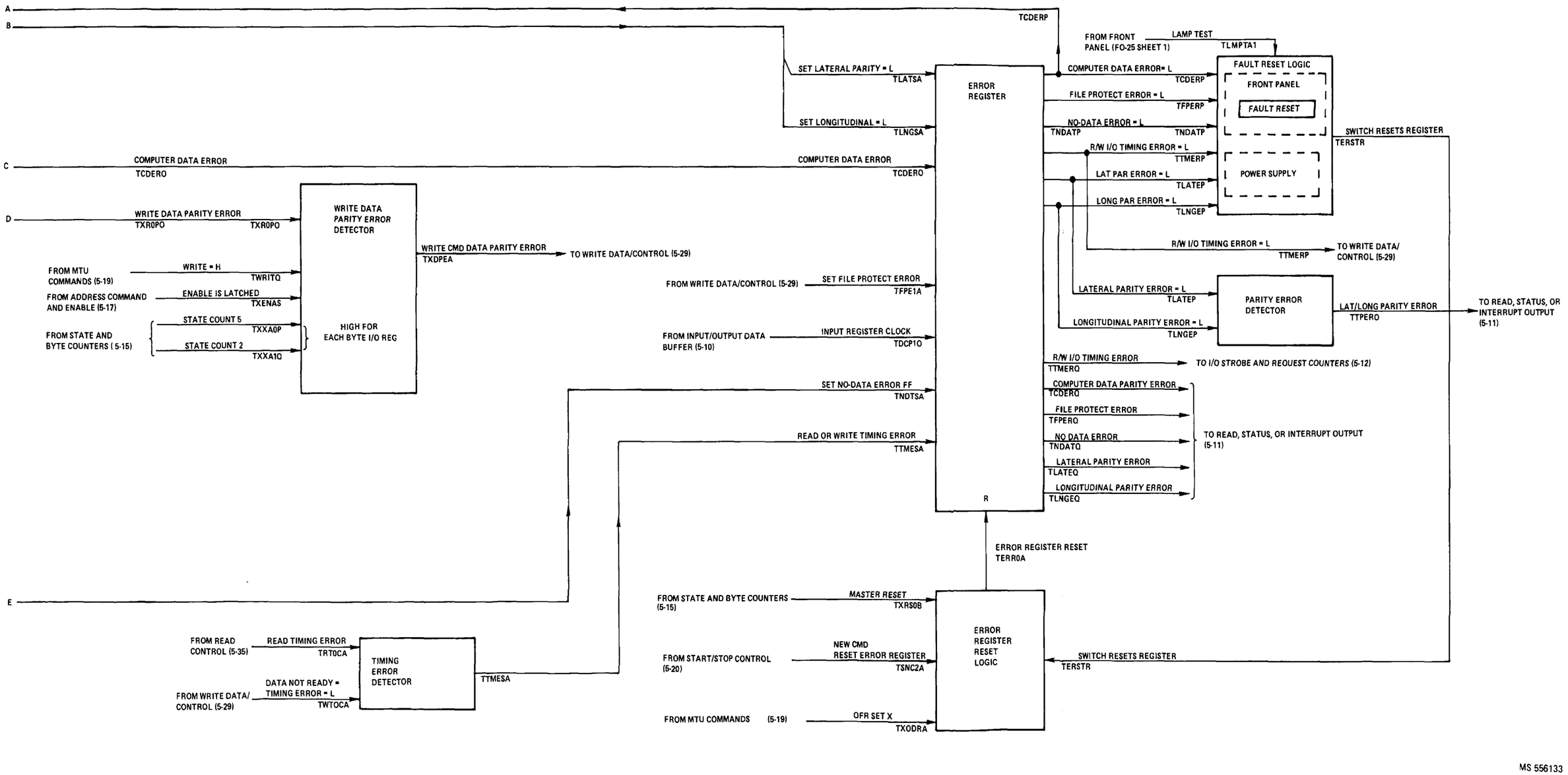
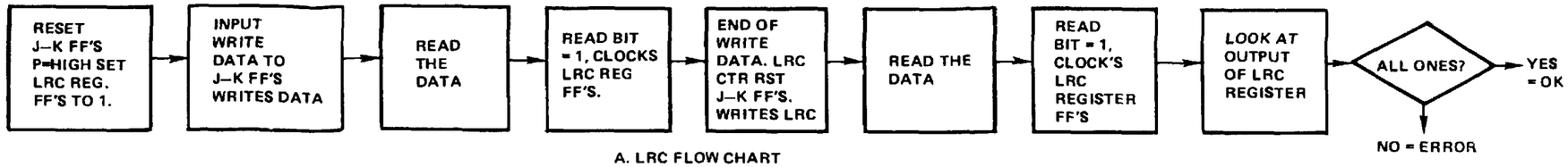
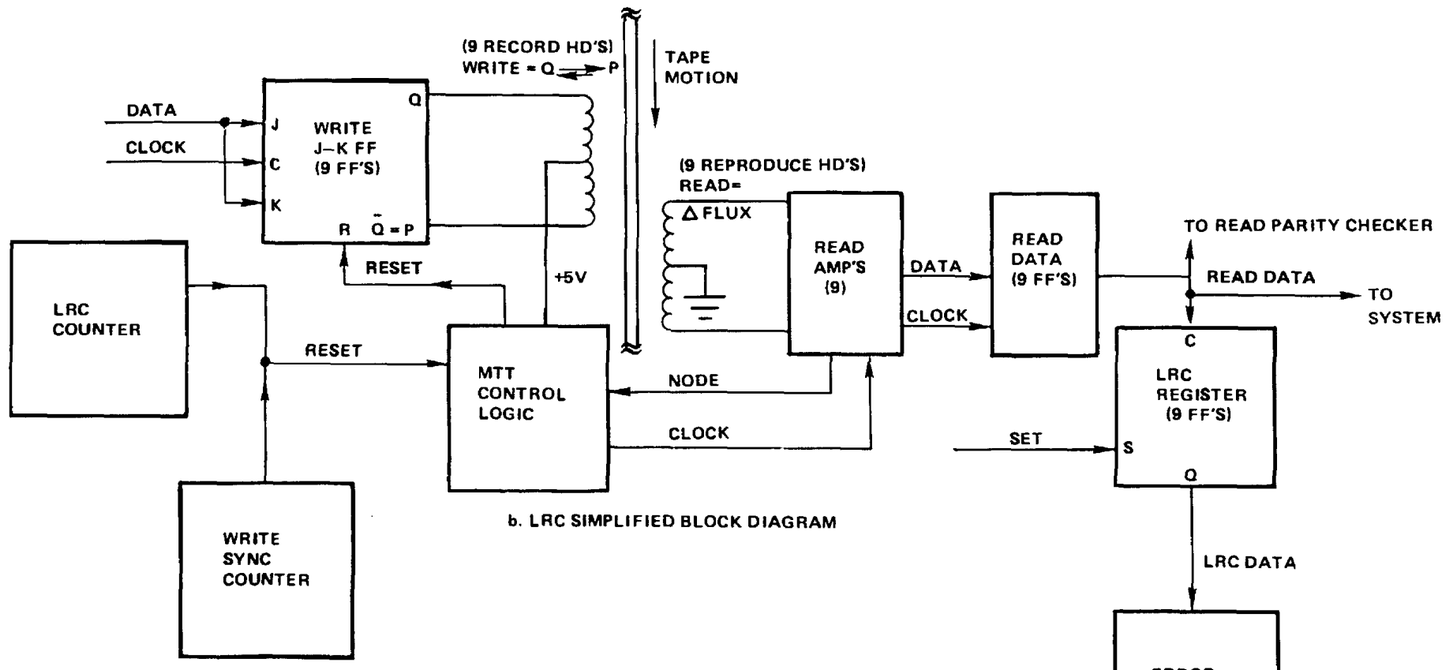


Figure 5-44. Error Detect Block Diagram (Sheet 2 of 2)



A. LRC FLOW CHART



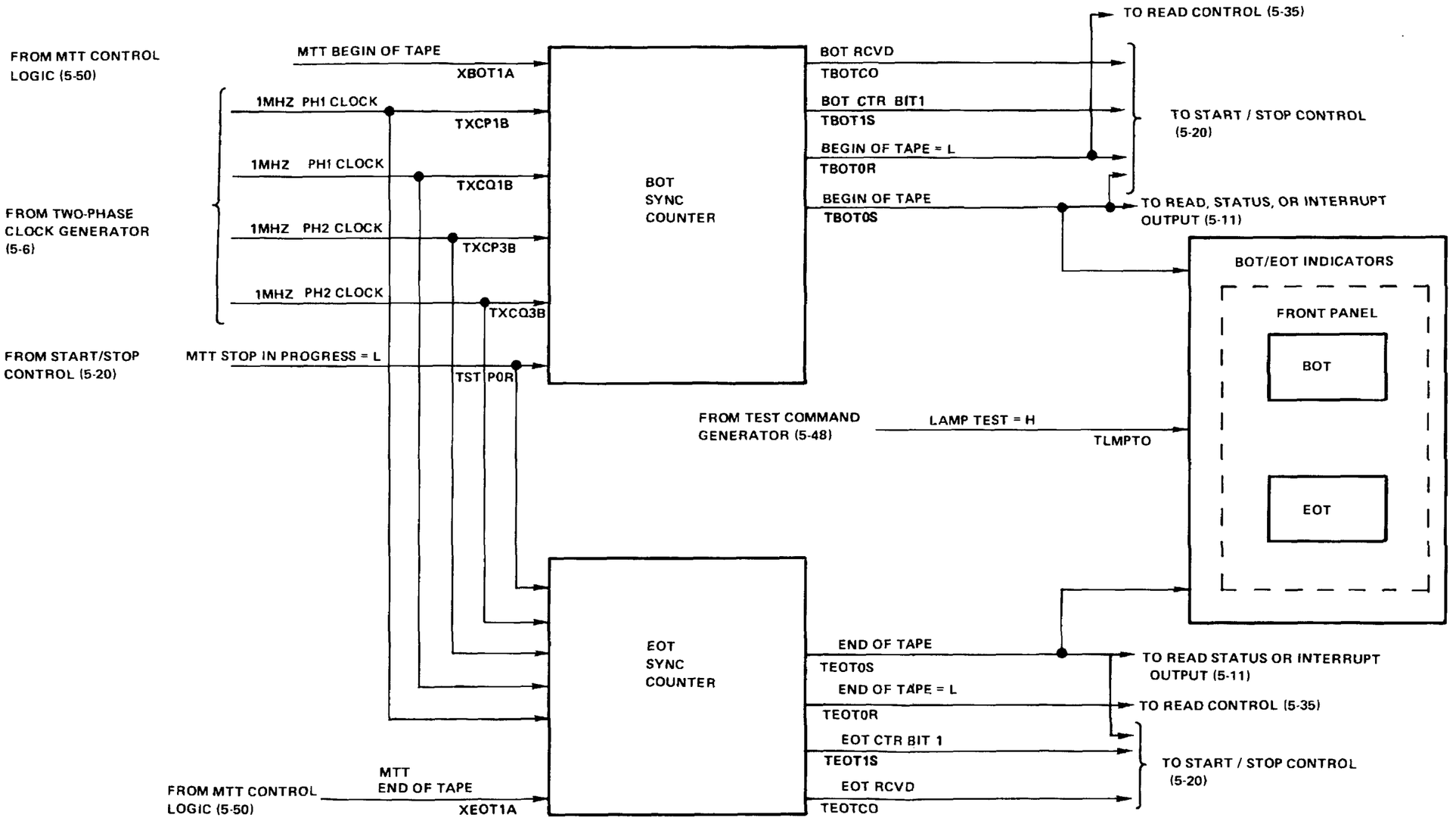
b. LRC SIMPLIFIED BLOCK DIAGRAM

C. AN EXAMPLE OF A WRITE AND LRC SEQUENCE SHOWING TWO BYTES OF WRITE DATA

SIGNAL	WRITE DATA (1 = HIGH, 0 = LOW)									WRITE J–K FF (HIGH = Q OR P)									READ DATA FF'S OUTPUT									LRC REG. Q OUTPUT								
BITS	1	2	3	4	5	6	7	8	P	1	2	3	4	5	6	7	8	P	1	2	3	4	5	6	7	8	P	1	2	3	4	5	6	7	8	P
RESET	0	0	0	0	0	0	0	0	0	P	P	P	P	P	P	P	P	P	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
1ST BYTE	0	1	1	0	1	0	0	0	1	P	Q	Q	P	Q	P	P	P	Q	0	1	1	0	1	0	0	0	1	1	0	0	1	0	1	1	1	0
2ND BYTE	1	1	0	1	1	0	0	1	1	Q	P	Q	Q	P	P	P	Q	P	1	1	0	1	1	0	0	1	1	0	1	0	0	1	1	1	0	1
LRC RST	0	0	0	0	0	0	0	0	0	P	P	P	P	P	P	P	P	P	1	0	1	1	0	0	0	1	0	1	1	1	1	1	1	1	1	1

MS 556134

Figure 5-45. Longitudinal Redundancy Check Block Diagram



MS 556135

Figure 5-46. BOT/EOT Detect Block Diagram

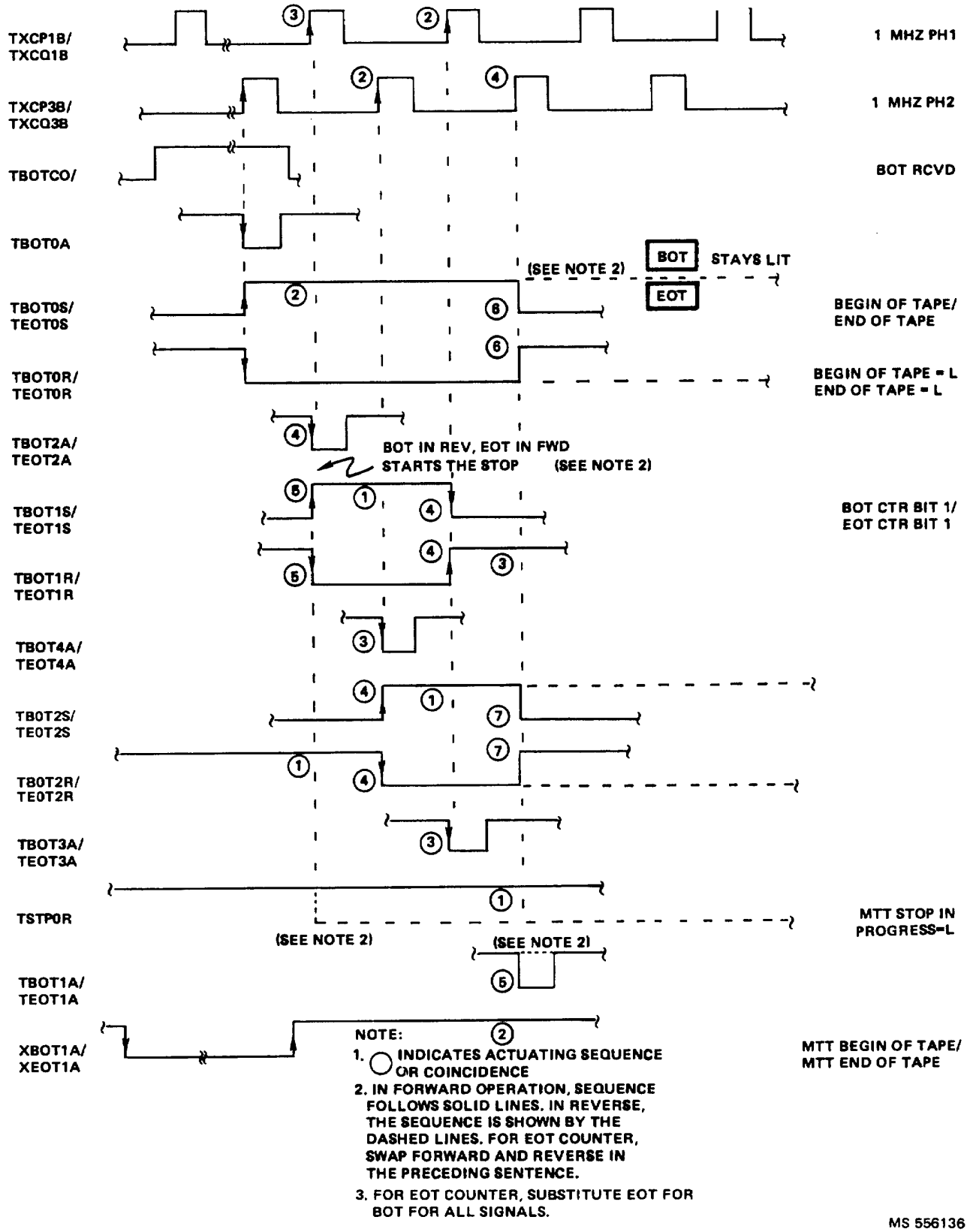


Figure 5-47. BOT/EOT SYNC Counters Timing Diagram

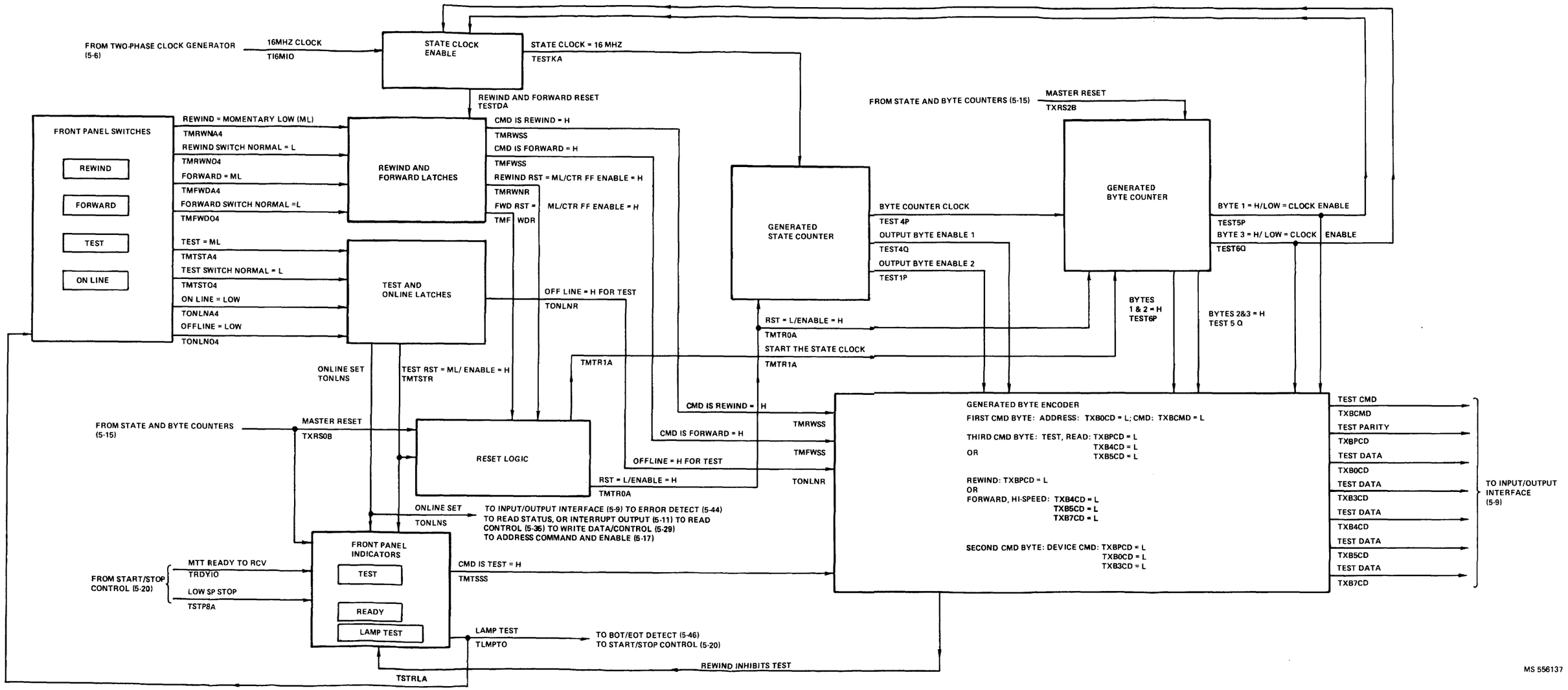


Figure 5-48. Test Command Generator Block Diagram

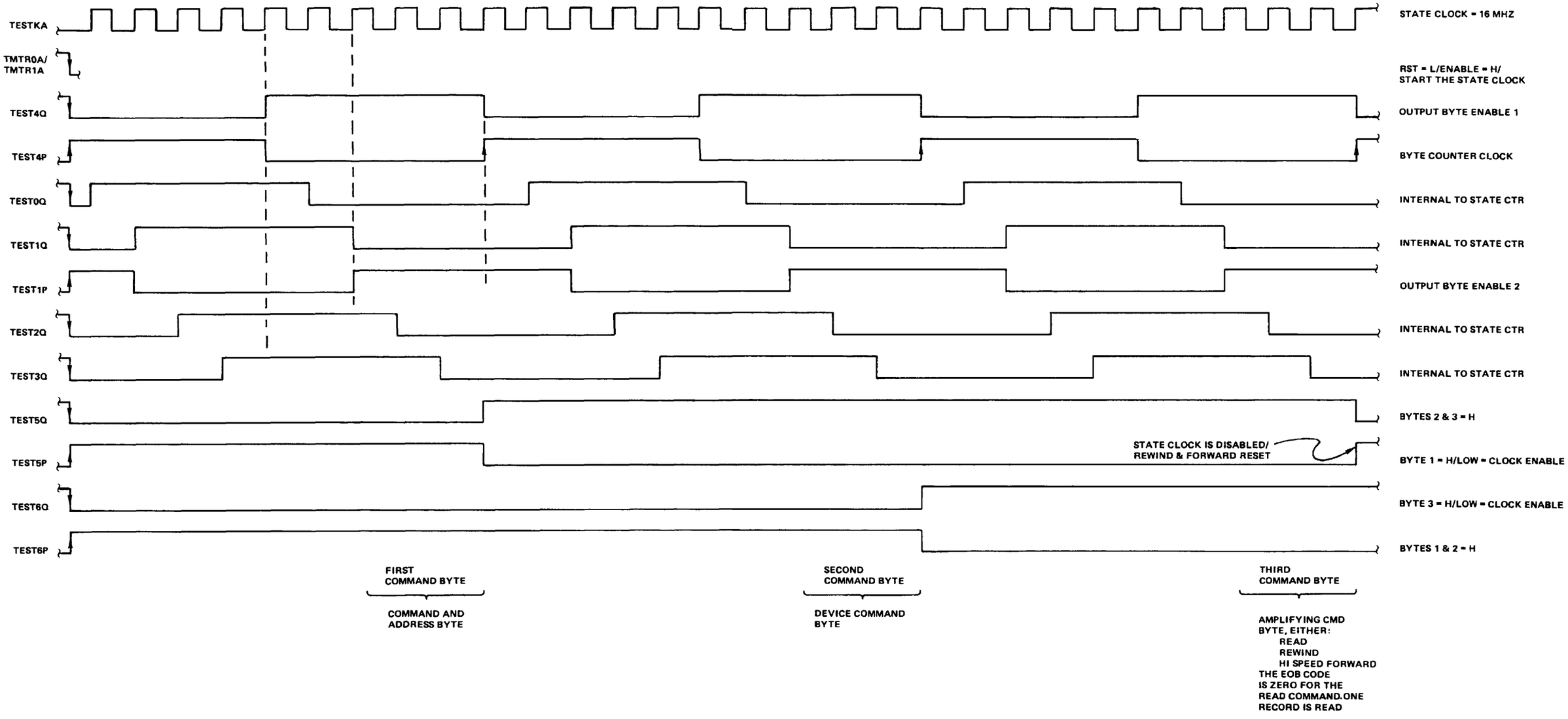


Figure 5-49. Test Commands Timing Diagram

the high TESTOQ. With TESTOQ high, the next clock produces the high TEST1Q and the low *output byte enable 2* signal (TEST1P). The high TEST1Q on the next clock produces the high TEST2Q. The high TEST2Q on the next clock produces the high TEST3Q. The high TEST3Q produces the *high output byte enable 1* signal (TEST4Q) and the low TEST4P. The low TEST4P on the next clock produces the low TESTOQ. The low TESTOQ on the next clock produces the low TEST1Q and the high *output byte enable 2* signal (TEST1P). The high *output byte enable 1&2* signals (TEST4Q and TEST1P) combine to satisfy enable logic for each of the three command bytes. The low TEST1Q on the next clock produces the low TEST2Q. The low TEST2Q on the next clock produces the low TEST3Q. The low TEST3Q on the tenth clock produces the low TEST4Q and the high TEST4P which clocks the byte counter to byte 2. This cycle of the state counter is repeated for the second byte and again for the third byte. At the completion of the third byte the TESTKA is disabled.

i. Generated Byte Encoder (fig. 5-48 and 5-49). The encoder produces the command and address code during the first byte for any one of the three possible commands; rewind, forward, and test. The encoder produces the device command code during the second byte for any one of the three commands. The encoder provides the output code for rewind when REWIND is selected; the output code for forward, high speed when FORWARD is selected; and the output code for read when TEST is selected. The output codes and the input conditional logic to produce them are shown in table 5-7. The timing to generate the logic for each byte code is shown in figure 5-49. The signal flow of the input timing logic and the selection logic for the third byte code is shown in figure 5-48.

5-28. MTT Control Logic (fig. 5-50). The MTT control logic is located on one printed circuit board A4 in the MTT subassembly. The purpose of this logic is to interface between the card cage assembly A2 and the MTT subassembly, and to provide interlocks that prevent operation of the tape cartridge in the MTT unless the necessary conditions are satisfied: e.g. cartridge in place (CIP) and door closed (DC). The interface consists of translating command signals to control signals, which go to the tape drive, read function, and write function and of providing ready status, EOT and BOT markers for the MTU assembly. The logic is subdivided into the following functions:

Rewind latch

Motor control

BOT latch

Ready logic

Output drivers

MTT read control

MTT write control

a. Rewind Latch (fig. 5-50). This function provides run commands (forward and reverse) that position the tape so that it is ready for any run forward command from the ADP. The rewind flop-flip (FF) set = L signal (XREWAD) is set low by either the high end hole = H signal (XENHOA) or the combination of the following signals:

(1) *Load point debounce flip-flop (FF) set=H* signal (XLPFFS) is high (function of actuating the REWIND switch on the MTT front panel).

(2) *Beginning of tape (BOT=H)* signal (XBOTAA) is low (not at BOT).

(3) The cartridge in place switch A8S3 is closed, which produces a low *cartridge in place=low* signal (XCPINT).

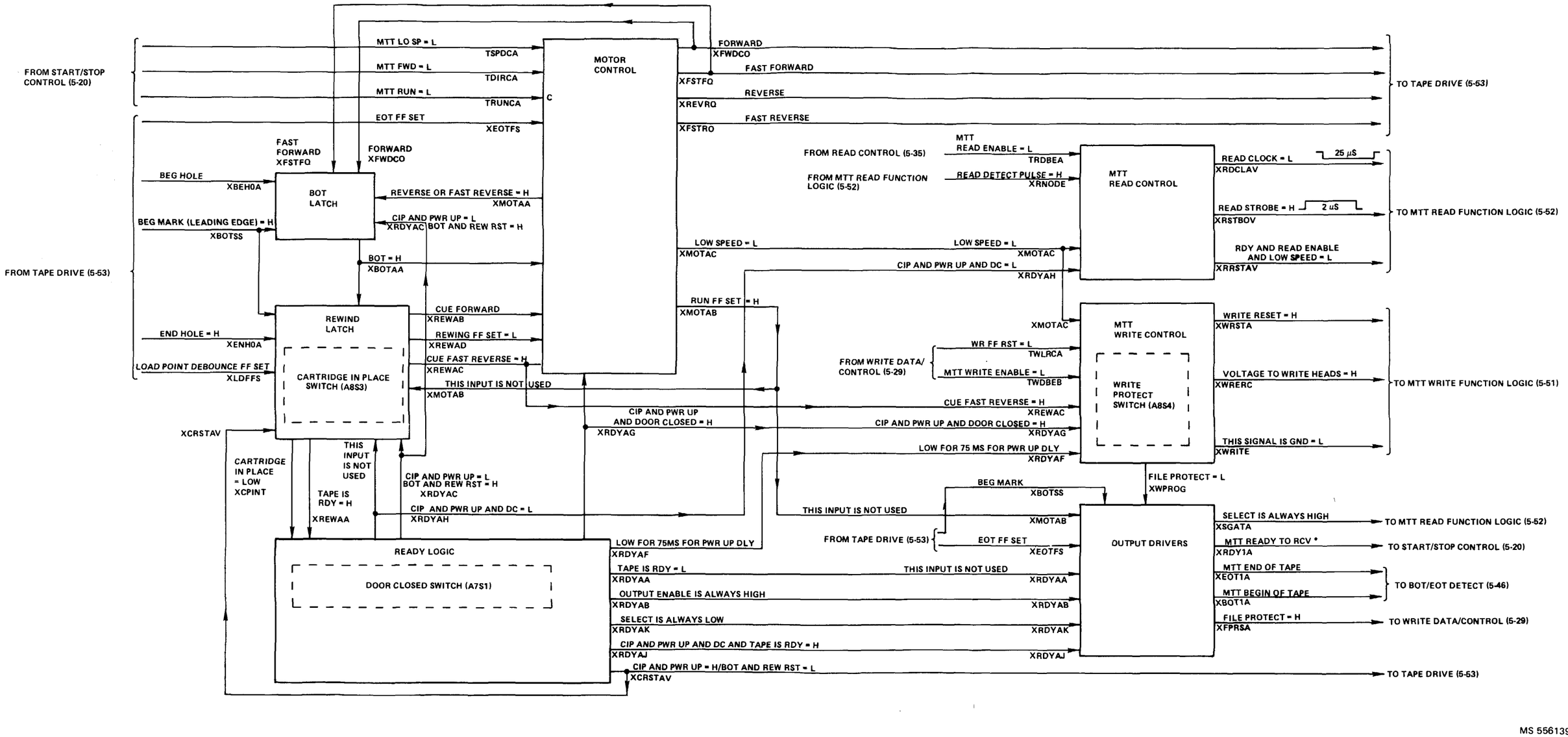
When the *rewind flip-flop (FF) set=L* signal (XREWAD) goes low, the *cue fast reverse=H* signal (XREWAC) goes high. The low XREWAD also goes to the motor control where it disables the ADP commands to the tape drive. The high XREWAC initiates the tape rewinding, which continues until the BOT marker is detected; this is indicated by the high XBOTAA. The high XBOTAA resets XREWAC to low and XREWAD to high. When XREWAC goes low, the tape coasts to a stop. When XREWAD transitions from low to high, it triggers a high 350ms one-shot pedestal internal to the function. During this 350-ms, the tape (moving in reverse) is allowed to continue coasting to a stop. At the completion of the 350-ms pedestal, the pedestal transition from high to low triggers the high 4-see one-shot *cue forward* output signal (XREWAB). The high XREWAB initiates tape movement forward at normal speed until the BOT marker is indicated by the high begin (BEG) *mark* low. With XREWAB, the 350-ms pedestal, and XREWAC all low, the tape is *ready* (RDY)=H output signal (XREWAA) is produced. Initially, before a cartridge is in place and during a 75-ms delay after power is turned on, the

Table 5-7. Generated Byte Encoder Truth Table

	First Byte (All)	Second Byte (All)	Third Byte (Select One)
		INPUTS	
		(1=High, 0=Low)	
TONLNR	1	1	1 1 1
TEST1P	1	1	1 1 1
TEST4Q	1	1	1 1 1
TEST5Q	0	1	1 1 1
TEST5P	1	0	0 0 0
TEST6Q	0	0	1 1 1
TEST6P	1	1	0 0 0
TMRWSS	X	X	1 0 0
TMFWSS	X	X	0 1 0
TMTSSS	X	X	0 0 1
		OUTPUTS	
		(1=Low, 0=High)	
TXBCMD	1	0	0 0 0
TXBPCD	0	1	1 0 1
TXB0CD	1	1	0 0 0 (Byte Data)
TXB3CD	0	1	0 0 0 (Byte Data)
TXB4CD	0	0	0 1 1 (Byte Data)
TXB5CD	0	0	0 1 1 (Byte Data)
TXB7CD	0	0	1 0 0 (Byte Data)
TSTRLA	0	1	1 0 0

NOTE:

X indicates these signals are not part of the input logic but at least one of the three signals must be present because of prior condition of selecting either rewind/forward or test.



MS 556139

Figure 5-50. MTT Control Logic Block Diagram

high cartridge in place and power up = low/beginning of tape and rewind reset = high (CIP and PWR UP = L/BOT and REW RST=H signal (XRDYAC) resets XREWAC and the 350-ms one-shot pedestal to low and XREWAD to high. At the same time, the low *CIP and PWR UP = HIBOT and REW RST = L* signal (XCRSTAV) resets XREWAB to low.

b. Motor Control (fig. 5-50). The motor control provides signals to the tape drive for controlling speed and direction of tape movement. The control signals are a result of run commands from the start/stop control and cue commands from the rewind latch described in the preceding paragraph. Only the run commands from the start/stop control are disabled when any one of the following conditions exist.

(1) *MTT run=L* (TRUNCA) is high.

(2) *MTT forward (FWD)= L* (TDIRCA) is high and *BOT=H* (XBOTAA) is high.

(3) *CIP and power delay (POOR DLY) and door closed=H* (XRDYAG) is low.

(4) *Rewind pip-pop (FF) set=L* (XREWAD) is low.

(5) *MTT FWD =L* (TDIRCA) is low and *end of tape flip-pop (EOT FF) set* (XEOTFS) is high. When XREWAD is low, the cue commands *cue forward* (XREWAB) and *cue fast reverse* (XREWAC) produce the respective *forward* (XFWDCO) and the *fast reverse* (XFSTRO) high output signals. When the run commands are enabled by the low *MTT run = L* signal (TRUNCA), the output signals are decoded as follows:

(6) (*MTT low speed (LO SP)=L* (TSPDCA) is low and TDIRCA is low) = *forward* (XPWDCO) is high.

(7) (TSPDCA is high and TDIRCA is low) = *fast forward* (XFSTFQ) is high.

(8) (TSPDCA is low and TDIRCA is high) = *reverse* (XREVRQ) is high.

(9) (TSPDCA is high and TDIRCA is high) = XFSTRO is high. When XREVRQ or XFSTRO goes high, the output to the BOT latch *reverse or fast reverse* (XMOTAA) goes high. The *run pip-pop (FF) set = H* signal (XMOTAB) goes high when TRUNCA goes low. Signal XMOTAB is sent to the rewind latch and to the output drivers. However, the signal is not used in those blocks. The connections are shown for completeness.

c. Beginning of Tape (BOT) Latch (fig. 5-50). The BOT latch function provides a gated or a latched signal output. When the *beginning (BEG) hole* (XBDHOA) signal goes high, the output signal *BOT=H* (XBOTAA) is latched high, or when the *beginning (BEG)* mark (leading edge) (XBOTSS) goes high, XBOTAA remains high as long as XBOTSS is high. Also, when the *reverse or fast reverse=H* signal (XMOTAA) is high and XBOTSS goes high, the *BOT=H* signal (XBOTAA) is latched high. The latch is reset in any one of four ways: (1) XMOTAA is low and XBOTSS goes high.

(2) *CIP and PWR up = LIBOT and REW RST=H* (XRDYAC) goes high.

(3) *Forward* (XFWDCO) is high and XBOTSS goes high.

(4) *Fast forward* (XFSTFQ) is high and XBOTSS goes high.

d. Ready Logic (fig. 5-50). The MTT is ready when the power delay has timed out, the cartridge is in place, the door for the cartridge is closed, and the tape is ready. The output signal *low for 75 ms for power (POOR) up delay (DLY)* output signal (XRDYAF) is low for 75 ms at initial turn on and then goes high as a capacitor within the block charges to full charge. With XRDYAF high, when the *cartridge in place=low signal* (XCPINT) *goes low, the cartridge in place and power up = L/ beginning of tape and rewind reset = H (CIP and PWR UP = LIBOT and REW RST = H)* output signal (XRDYAC) goes low. The low XRDYAC produces the high *CIP and PWR up = HIBOT and REW RST = L* output signal (XCRSTAV). The *select is always low* output signal (XRDYAK) is hardwired to produce a constant low. With XRDYAC and XRDYAK both low, DOOR CLOSED switch A7S], when actuated, produces the high *CIP and power delay (POOR DLY) and door closed =H* output signal (XRDYAG). The high XRDYAG produces the low *CIP and power (POOR) up and door close (DC)=L* output signal (XRDYAH). The *tape is ready (RDY)=H* signal (XREWAA), when high, produces the low *tape is RDY=L* output signal (XRDYAA). The low XRDYAA and the low XRDYAH produce the high *CIP and PWR up and DC and tape is RDY=H* output signal (XRDYAJ). The low signal XRDYAK is inverted to produce the high *output enable* is *always high* output signal (XRDYAB).

e. Output Drivers (fig. 5-50). The drivers are enabled constantly by the *output enable is always high* signal (XRDYAB). The *tape is ready (RDY)=L* input signal (XRDYAA) does not provide a useable output from the output drivers. The *select is always*

low signal (XRDYAK) is inverted, in effect, to produce the *select is always high* output signal (XSGATA). The *CIP and PWR up and DC and tape is RDY=H* signal (XRDYAJ) produces the low *MTT ready to receive (RCV)** output signal (XRDY1A). The *high end of tape flip-pop (EOT FF) set* (XEOTFS) *and beginning (BEG) mark* (XBOTSS) signals produce, respectively, the low *MTT end of tape* (XBOT1A) and *MTT begin of tape* (XBOT1A) output signals. The *run flip-flop (FF) set=H* signal (XMOTAB) does not provide a useable output from the output drivers. The low *file protect=L* signal (XWPROG) produces the high *file protect = H* signal (XFPRSA) (for writing, XFPRSA is low). The unused connections are shown for completeness.

f. M7T Read Control (fig. 5-50). The MTT read control provides a read clock of sufficient pulse width for each byte of data detected on the tape so that synchronization with the MTU clock is assured. The MTT read control also provides two other outputs for control of the read data. Initially, with the *cartridge in place and power up and door closed = L (CIP and PWR up and DC = L)* signal (XRDYAH) low, when the *MTT read enable = L* signal (TRDBEA) goes low, the *read clock=L* signal (XRDCLAV) is reset high and the *read strobe=H* signal (XRSTBOV) is reset low. With XRDYAH and TRDBEA low, when the *low speed = L* signal (XMOTAC) goes low, the *ready (RDY) and read enable and low speed =L* output signal (XRRSTAV) goes low. With the tape moving, when data is *read from the tape, the read detect pulse = H* signal (XRNODE) goes high, triggering the low 14.6to 23**µ**s *read strobe=L* signal pedestal (XRDCLAV). The low to high transition of the trailing edge of the *read strobe=L* signal pedestal (XRDCLAV) triggers a 5,**µ**s one-shot (internal to the block). After 5**µ**s, the high to low transition of the trailing edge of the 5**µ**s pedestal triggers the high 1.1**µ**s pedestal, which is the *read clock = H* output signal (XRSTBOV).

g. M17 Write Control (fig. 5-50). The write control provides a reset signal that resets the write flip-flops prior to a write operation and at the completion of a write operation. The write control also provides a voltage to the write heads when the MTT is ready and enabled. The *voltage to write heads = H* output signal (XWRERC) goes to approximately 4.5v when the following logic conditions are satisfied and write protect switch A8S4 is activated.

(1) XRDYA& is high.
(2) XRDYAF is high.
(3) MTT *write enable=L* (TWDBEB) is low.
(4) *Cue fast reverse=H* (TREWAC) is low.
(5) *Low speed=L* (XMOTAC) is low.

When write protect switch A8S4 returns to its normally closed position or any one of the five conditions just listed change state, or when the *write flip-flop reset (WP FF RST) = L* signal (TWLRCA) goes low, *the write reset = H* output signal (XWRSTA) goes high. The *this signal is GND=L* output signal (WRITE) provides a ground for the MTT write function from the MTT control logic.

5-29. MTT Write Function Logic (fig. 5-51). The MTT write function logic is located in the MTT. The pupose of this logic is to drive the write heads in accordance with the input write data. This function is subdivided into two blocks, one with nine write JK flip-flops and the other with nine write heads. There are 8 data bits and 1 parity bit for a total of 9 bits that must be recorded on nine separate channels. Each channel consists of a write JK flip-flop and a write head. The blocks are shown with all inputs. The following description is for the bit 1 channel, only.

a. Write JK Flip-Flops (fig. 5-51). When a byte of write data is present, at least one of *the MTT WP data=L* bits (TWDBOA through TWDB7A) or the *parity = L* bit (TWDBPA) must be low when the *write strobe=L* signal (TWDBSA) goes low. Initially, prior to the recording of data, the flip-flops are reset by *the write reset=H* signal (XWRSTA). When reset, the XWCH1H is low and XWCH1L is high. This provides the reference starting condition of the-flip-flop for the longitudinal redundancy check (LRC) reset (XWRSTA goes high), which occurs 390 ps after the last byte of a record. With the flip-flop reset initially, when bit 1 (TWDBOA) is low, the *write strobe=L* signal (TWDBSA) clocks the bit through the flip-flop, which forces XWCHIH to high and XWCH1L to low. Subsequent bytes, which produce a true low bit 1 (TWDBOA) when TWDBSA goes low, cause XWCH1H and XWCH1L to change state. This toggling of XWCH1H and XWCH1L occurs every time a clock occurs when the input is true. At 390 **µ**s, after completion of the record, XWRSTA goes high, resetting XWCH1H to low and XWCH 1 L to high. If there has been an even

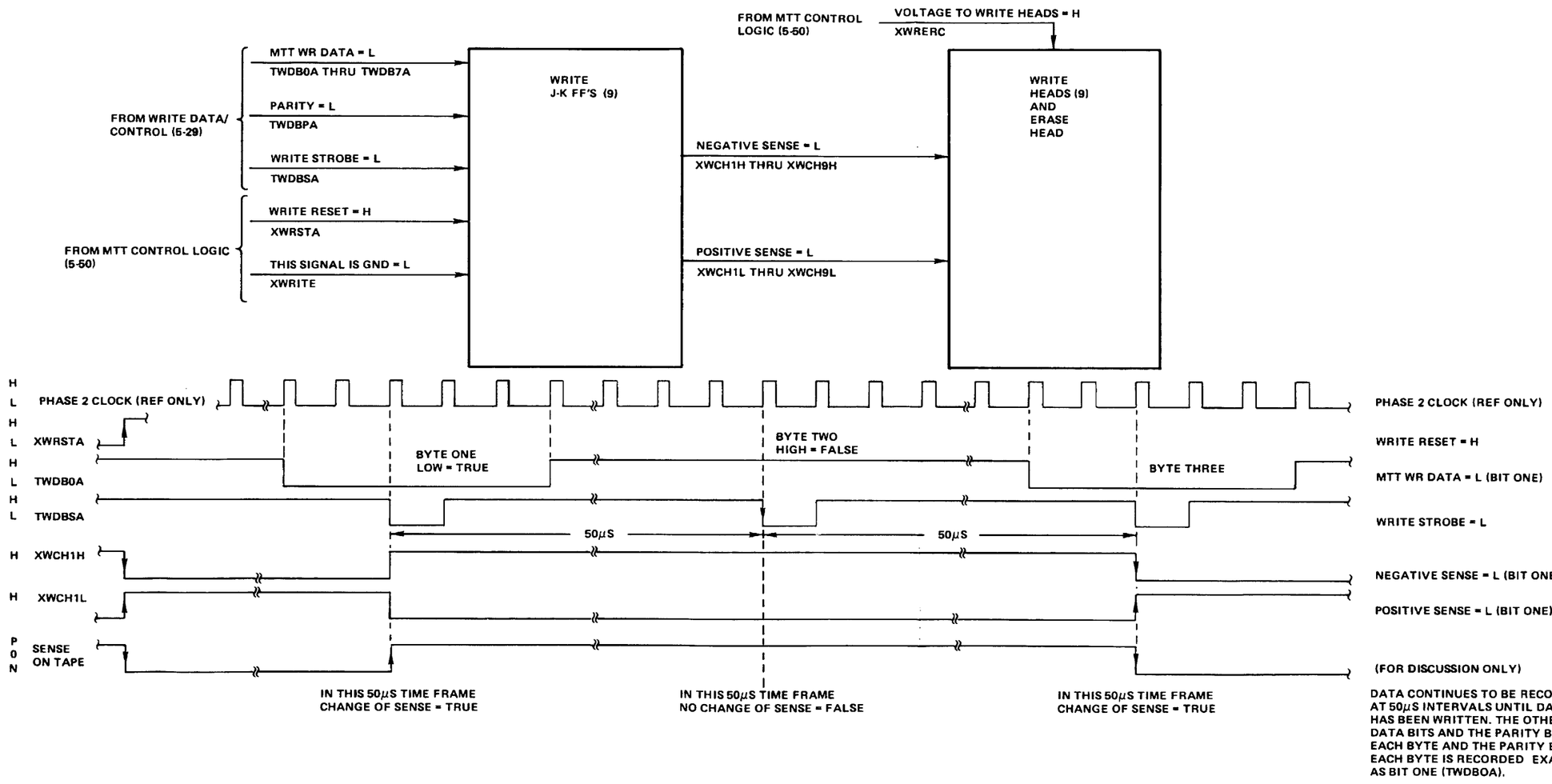


Figure 5-51. MTT Write Function Block Diagram

number of toggles during the length of the record, when reset occurs, there is no change of state for XWCH1H and XWCH1L. If there has been an odd number of toggles, XWCH 1 H and XWCH 1 L change state. Each toggle causes a logic 1 (1=true) to be written by the write head.

b. Write Heads arid Erase Head (fig. 5-51). The write heads are center-tapped coils with voltage applied to the center tap and a return alternately applied to one end or the other to drive current through the head in opposite directions. The coils do not have voltage applied at all times. The heads are enabled when the MTT control logic supplies the *voltage to write heads = H* signal (XWRERC). For the purpose of this description, a positive and negative sense has been assigned to the alignment or the ferrous material on the tape. Initially, the low signal XWCHIH causes current to flow through the head, generating a magnetic field that aligns the magnetic domain of the ferrous material on the tape to a negative sense. When an input bit causes XWCHIH to go high and the signal XWCHIL to go low, current flows through the head in the opposite direction. This produces an opposing magnetic field, which aligns the magnetic domain of the ferrous material on the tape to the positive sense. This change in sense is an indication that a logic l (l=true) has been recorded. Any subsequent byte could also contain a logic l for bit 1. If it does, XWCH 1 L goes high and XWCH 1 H goes low and the direction of the head current changes producing a change in the sense from positive to negative. This change in sense is also an indication that a logic 1 has been recorded. Therefore, a change of sense from either positive or negative is an indication that a logic 1 has been recorded. The erase head is energized when the write heads are enabled by the same enabling signal (XWRERC). The erase heads, therefore, are always energized when the write heads are being used. Consequently, the erase heads must be located in front of the write heads. This results in the tape being freshly erased prior to recording the write data.

5-30. MTT Read Function Logic (fig. 5-52). The MTT read function is located on three boards within the MTT. There are three identical circuits on each board, which makes a total of nine parallel channels; one each for the 8 bits of the data byte and the parity bit. The purpose of these circuits is to transform the nine possible simultaneous transitions of magnetic flux of each recorded byte on the tape to TTL logic levels and transfer the logic levels in parallel at precisely the same time, which realigns any of the 9 bits that may have become skewed during the recording and reproducing process. This discussion is subdivided into the blocks for read heads and amplifiers (fig. 5-52a) and the simplified schematic (fig. 5-52c) which discusses only one amplifier typical of the other eight.

a. Read Heads and Amplifiers (fig. 5-52a and 5-52b). In the read amplifier, the high *RDY and read enable and low speed=L* signal (XRRSTAV) resets the *L= read data with parity* signals (XRDBOA through XRDB7A with XRDBPA) to high. The high XRRSTAV also establishes the positive reference for the read amplifier so that every read operation for all nine channels always begins from the same reference. This is in coordination with the MTT write function that always resets the write flip-flops prior to recording any data. When XRRSTAV goes low, the read function is in operation. From the read heads, the nine *parallel read is true = NEG/POS* signals (XRCHIL through XRCH9L) are initially negative as a result of the recording process where the write flip-flops are reset. This produces a negative sense on the magnetic tape. For this discussion, only bits 1 and 2 are explained; the other 7 are identical. When the sense changes to positive for bit 1, the read head output (XRCH1L) transitions from negative to positive. After some delay through the amplifier, the *read detect pulse=H* signal (XRNODE) is pulsed high as a result of the negative to positive transition. Signal XRNODE goes to the MTT control logic where it initiates the active low 25**µ**s *read clock=L* signal (XRDCLAV). The low to high transition of the trailing edge of XRDCLAV results in the active low output signal XRDBOA. During the second byte, XRCH1L transitions from positive to negative, which also results in XRNODE. Signal XRNODE results in XRCLAV, which results in the output XRDBOA remaining low for the second byte. During the third byte, XRCH1L does not transition (data = false); however, XRCH2L does transition from negative to positive, which results in XRNODE. A transition of any of XRICH1L through XRCH9L produces XRNODE. Again, XRNODE results in XRDCLAV; the trailing edge forces XRDBOA high and XRDB1A low. During the fourth and last byte, both XRCH1L and XRCH2L transition to produce XRNODE, which results in XRDCLAV, which forces both XRDBOA and

XRDB1A low. In effect, this eliminates any time difference between these 2 bits of the fourth byte that may exist due to tape skew. The active high 2-**µ**s read strobe = H signal (XRDSTBOV) is, in effect, inverted to produce the L= read strobe output signal (XRDBSA). The select is always high signal (XSGATA) provides a constant output enable for XRDBOA through XRDB7A with XRDBPA and XRDBSA. Signals XRCH1H through XRCH9H are not used; they have been shorted out of the circuit by the placement of the grounds on the specific circuit elements.

b. Read Function Simplified Schematic (fig. 5-52c). The negative sense on the tapes, established routinely by the reset of the write flip-flop prior to any recording, induces a current in the read head in the direction that generates a negative voltage of about 15 mv p-p on the inverting input of the first integrating operational amplifier, which has. a voltage gain of about 200. The positive output is applied to the inverting input of the second integrating operational amplifier. The negative output is applied to the inverting input of the third operational amplifier, which has a reference (either positive or negative) applied through a regenerative feedback circuit to the noninverting input. Initially, the high XRRSTAV input to the noninverting input causes the output to go positive, which establishes a positive reference of about +0.8v; therefore, the negative input has no effect on the output. When the magnetic Rux on the tape transitions from negative to positive, induced head current reverses, generating a positive voltage, which is inverted twice and applied to the inverting input of the third operational amplifier. When the input positive voltage to the third operational amplifier exceeds the +0.8v threshold, the output goes negative. The regenerative feedback immediately forces the operational amplifier to saturation, creating a sharp drop in the output from maximum positive to maximum negative. This maximum negative establishes the -0.8v reference at the noninverting input. The next transition produces a negative voltage that exceeds the -0.8v reference forcing the output to saturation in the positive direction. The output is a square wave that is centered at -0.8v. The output is clamped to ground by a diode with its anode at ground potential. The resultant square wave to the delay and the exclusive OR (XOR) gate varies from 0v to approximately +11v. Initially, both inputs to the XOR gate are at the same level, which is high, and its output is low. At the first transition from positive to zero voltage, the undelayed input goes low and the XOR output goes high. After the delay, the other input goes low and the XOR output low. The high XOR output is equal to the delay and occurs for every transition of the input bit. The high XOR output is available to the output of this function through a diode, which is ORed with the other eight amplifier circuits to produce XRNODE. The high output of the XOR gate also sets the first flip-flop. Then, 25,us later, the low to high transition of the trailing edge of XRDCLAV clocks both flip-flops: Q1 to low and Q2 to high, since Q1 was set high. The output NAND gate is always enabled by XSGATA; so when Q2 goes high, XRDBOA goes low (low = true). Signal XRSTBOV produces XRDBSA.

5-31. MTT Tape Drive Electronics (fig. 5-53). The MTT tape drive electronics consists of analog and logic circuits within the MTT. The analog circuits consist of the servo amplifier, power amplifiers, motor-tachometer, and sensors that detect the beginning and ending of the magnetic tape. The logic consists of the FWD-RUN-EOT-Alert logic, the rewind-debounce latch, and the low tape/BOT/ EOT logic. The functional description is subdivided into the following areas:

Servo system

- Servo amplifier with ramp generator
- FWD and REV power amplifiers
- Capstan motor assembly

Tape sensors and logic

- Low tape/(BEG or end)/reflecting strip sensors
- Low tape/BOT/EOT logic

FWD run EOT alert

- Rewind debounce latch

a. Servo System (fig. 5-53). The servo system is a constant motor velocity servo system. It consists of the servo amplifier with ramp generator, the forward (FOOD) and reverse (REV) power amplifiers, and the capstan motor assembly. The capstan motor assembly consists of a motor and a tachometer generator. The motor turns either forward or reverse at either fast or normal speed. Speed is controlled by an error drive signal that controls the FWD or REV power amplifier by supplying current to the motor. The input command to the servo system selects the polarity and amplitude of the input to the ramp generator of the servo amplifier. The ramp generator produces the ramped drive

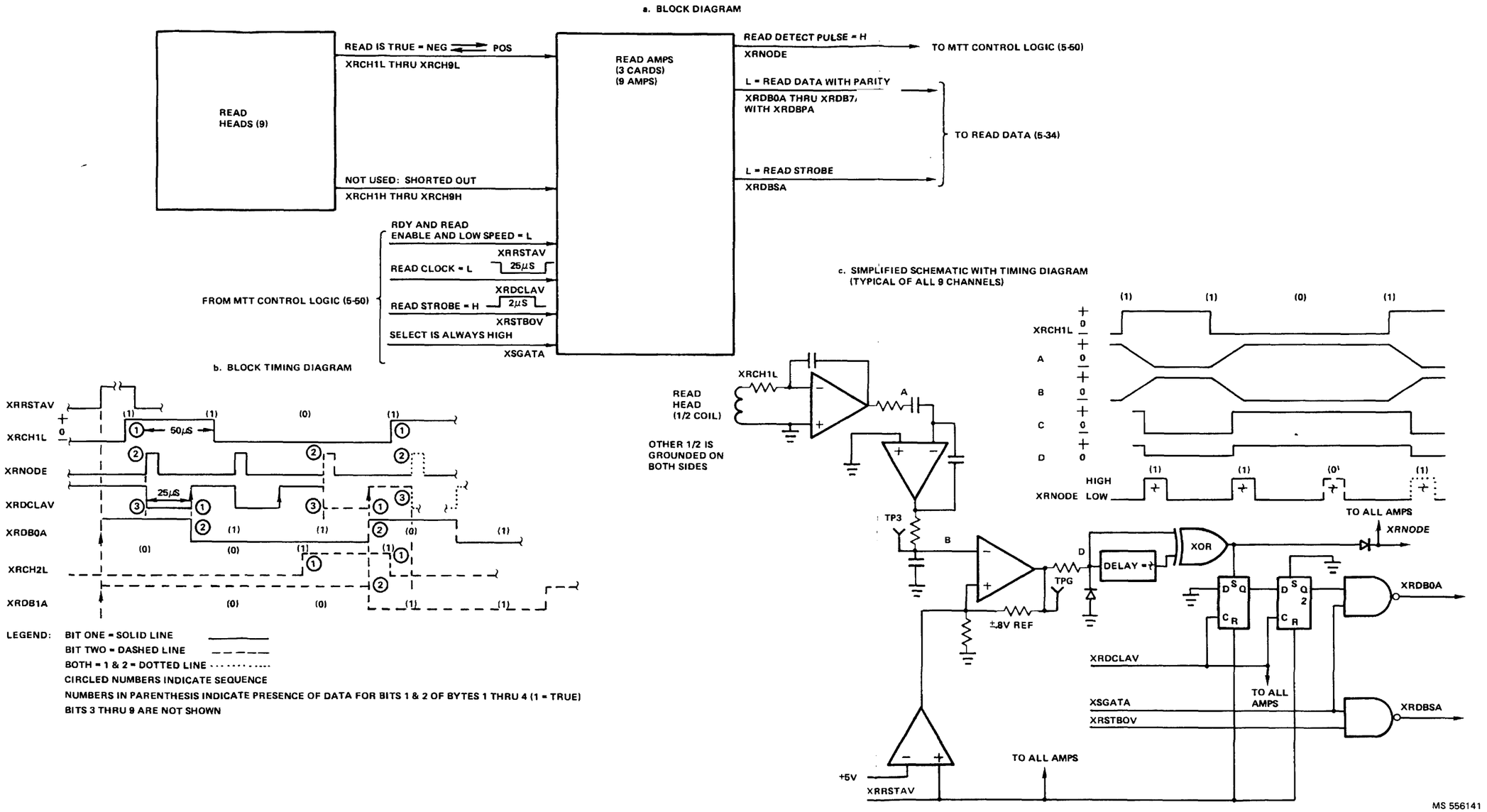


Figure 5-52. MTT Read Function Block Diagram

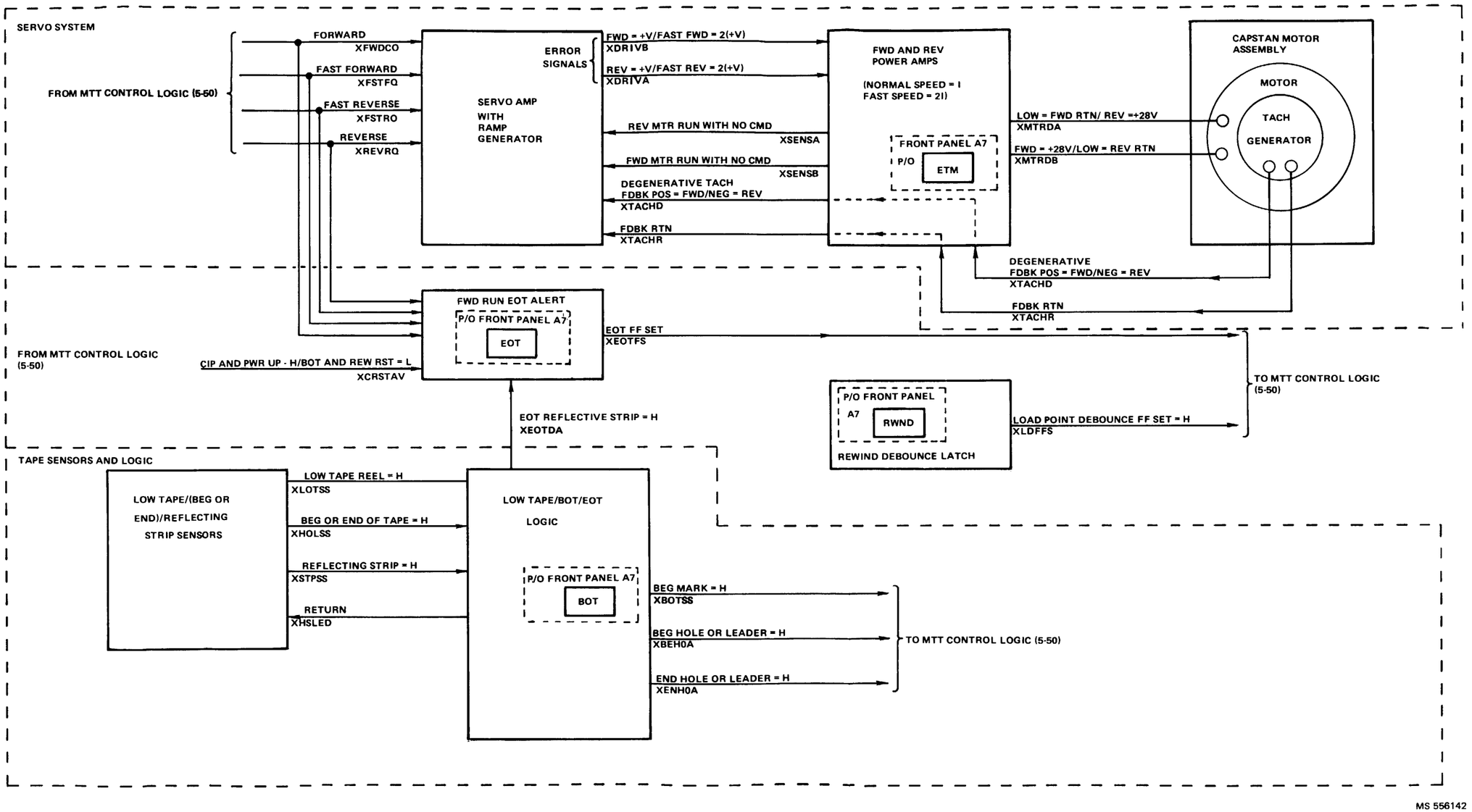


Figure 5-53. MTT Tape Drive Electronics Block Diagram

signal. In the motor assembly, attached to the motor, is the tachometer generator that generates an output that is fed back degeneratively to the servo amplifier. The feedback reduces the ramped drive signal. This creates the error drive signal from the servo amplifier that controls either the FWD or REV power amplifier. An unwanted increase in the magnitude of the error drive signal as a result of less drag on the motor attempts to drive the motor faster, but the generator output increases. This increase in feedback reduces the motor drive error signal, which maintains a constant motor speed. Conversely, an unwanted decrease in the magnitude of the error drive signal as a result of more drag on the motor attempts to slow the motor, but the generator output decreases and the error drive signal increases, which also causes the motor to maintain its constant speed. This process creates a motor velocity servo. With no command input, the motor might have some undesired motion due to leakage current in one or the other of the FWD or REV power amplifiers. This is prevented by tapping off a sense voltage from the return line of each of the amplifiers and feeding it back to the servo amplifier. The sense polarity is such that the line used for the error drive signal now carries a voltage that biases to cutoff the amplifier that produces it. Therefore, the motor does not turn unless there is a run command.

(1) *Servo amplifier with ramp generator*. When any one of the *forward* (XFWDCO), *fast forward* (XFSTFQ), *fast reverse* (XFSTRO), or *reverse* (XREVRQ) signals go high, a selected reference voltage level (polarity determines direction, magnitude determines speed) is switched to the ramp generator, which produces a motor drive voltage that increases in magnitude over time. This drive voltage, with no feedback from the tachometer generator, becomes either the *FWD= ±V/fast FWD=2(±V)* (XDRIVB) signal or the *REV= ±V/fast REV = 2(± V*) (XDREVA) signal. This allows the motor to begin rotating slowly and come up to operating speed at a rate determined by the ramp time (approximately 18 ms). As the motor turns the tachometer generator, the *tachometer feed back degenerative (tach FDBK)POS = FWD/NEG = REV* signal (XTACHD) reduces either the signal XDRIVB or XDRIVA, which depends on the motor run direction. When there is no run command, if the *reverse motor (REV MTR) run with no command (CMD)* signal (XSENSA) goes positive, the signal XDRIVA goes negative, which cuts off XSENSA. If the *forward motor (FWD MTR) run with no CMD* signal (XSENSB) goes positive, XDRIVB goes negative, which cuts off XSENSB.

(2) *Forward (FWD) and reverse (REV) power amplifiers*. The positive XDRIVB turns on the FWD power amplifier. The FWD power amplifier produces the *FWD= ±28v* (XMTRDB) and *low = FWD RTN* (XMTRDA) output signals. The *REV= ± V/fast REV= 2(± V*) positive signal (XDRIVA) turns on the REV power amplifier. The REV power amplifier produces the REV= ±28v (XMTRDA) and *low-= REV RTN* (XMTRDB) output signals. Signals XDRIVB and XDRIVA, when the run command is for fast speed, are amplified by the power amplifiers to produce twice the current through XMTRDB and XMTRDA as when normal speed is commanded. Unwanted leakage current through the REV power amplifier, the motor, and the return produces a positive XSENSA. The same condition in the FWD power amplifier produces a positive XSENSB.

(3) *Capstan motor assembly*. The motor rotates, moving the tape in the forward direction when XMTRDB is positive and XMTRDA is low. The polarities are reversed for the reverse direction. The current through these two lines is doubled for the fast run commands. The tachometer generator is attached to the motor and generates a voltage when the motor turns. When rotating forward, the generator generates a positive voltage. When rotating in the reverse direction, a negative voltage is generated. The resulting negative feedback signal is XTACHD. The voltage return is the FDBK RTN (XTACHR) signal.

b. Tape Sensors and Logic (fig. 5-53). The purpose of this function is to provide beginning (BEG) and ending markers. This function is subdivided into two blocks; low tape/(BEG or end)/reflecting strip sensors and low tape/beginning of tape (BOT)/ end of tape (EOT) logic. There are three sensor outputs that work in combination to logically produce the tape beginning and ending markers.

(1) *Low tape/(BEG or end)/reflecting strip sensors*. When the roll of tape on the reel reaches a level that allows the light emitted by an LED to be received by a light sensitive transistor on the other side of the reel, the *low tape reel = H* signal (XLOTSS) goes high. When either the BEG hole or leader on the tape, or the end hole or leader on the tape passes between another LED and its light sensitive transistor, the signal BEG *or end of*

tape =H (XHOLSS) goes high. A reflecting strip at either end of the tape reflects light emitted from the LED back to another light sensitive transistor, which produces the high *reflecting strip = H* signal (XSTPSS). The return line for the LED's is the signal *return* (XHSLED).

(2) *Low tape/BOT/EOT logic*. When XLOTSS and XSTPSS are both high, the *EOT reflective strip = H* output signal (XEDTDA) goes high. When XLOTSS and the BEG *or end of tape = H* signal (XHOLSS) both go high, the *end of hole or leader = H* output signal (XENHOA) goes high. When XLOTSS is low and XHOLSS goes high, the BEG *hole or leader = H* output signal (XBEHOA) goes high. When XLOTSS is low and XSTPSS goes high, the BEG mark = H output signal (XBOTSS) goes high. The BOT indicator lights when XBOTSS goes high.

c. Forward (FWD) Run End of Tape (EOT) Alert (fig. 5-53). The FWD run EOT alert logic produces an alert that the end of tape is near when running fast or normal in the forward direction. This is accomplished by the following logic. When either the *forward* sign

al (XFWDCO) or the *fast forward* signal (XFSTFQ) is high and the *EOT reflective strip = H* signal (XEOTDA) goes high, the *EOT FF set* output signal (XEOTFS) goes high. The EOT indicator lights when XEOTFS goes high. Signal XEOTFS is reset low when either the *reverse* signal (XREVRQ) or the *fast reverse* signal (XFSTRO) is high and XEOTDA goes high. Signal XEOTFS is also reset low by the *CIP and PWR UP = H/BOT and REW RST= L* (XCRSTAV) signal when it goes low.

d. Rewind Debounce Latch (fig. 5-53). The debounce latch is set when the RWND switch on the MTT front panel is pressed, and it is reset when the switch is released. The output signal is *load point debounce FF set = H* (XLDFFS).

Section IV. WIRING HARNESS AND POWER DISTRIBUTION

5-32. W2 Harness and Front Panel Wiring Diagram (Volume 3, FO-25). This drawing shows the wiring for all the switches and indicators on the from panel and the W2 connections between power supply PSI, card cage A2, and the magnetic tape transport (MTT) A I as well as the connection to the TSQ-73 system. The distribution for the signals on this diagram are shown in the key signal lookup table.

5-33. MTT Wiring Diagram (Volume 3, FO-26). This drawing shows the connections within the MTT between MTT power supply PS1, line filter FL1, tape deck assembly A8, power servo assembly A9, front panel assembly A7, and interface board A10. Interface board A10 contains MTT control logic printed circuit board A4; three read/write amplifier printed circuit boards A1, A2, and A3; servo amplifier A5; and read/write/erase head PU1. The connectors to magnetic tape unit (MTU) card cage A2 and MTU power supply PS1 are also shown. The distribution for signals on this diagram is shown in the key signal lookup table.

5-34. W1, W3, and Module Test Set (MTS) Interface Wiring Diagram (Volume 3, FO-27). This drawing shows all of the connections jumpered by the MTS interface card when it is installed. The card is removed when the MTU is tested by the MTS and power is connected to the plug from the MTS. The W1 and W3 cables are also shown. The distribution of signals appearing on this drawing can be found in the key signal lookup table. Power disconnected when the MTS interface card is removed is shown in volume 3, FO 5-2B.

5-35. Power Distribution (fig. 5-54). Power supply PSI supplies dc voltages of +5, -5, + 12, and +30 to card cage A2. The +30v is fed through the card cage to MTT A1. With + 135v applied, the auxiliary converter within PS1 produces dc voltages of -5, +5, and +25. These voltages are applied to the switch and control circuits of PS1. With these voltages applied to the switch and control circuits, when POWER switch S1 on the front panel is activated, transistor Q1 is turned on and the + 135v is applied to the primary of the main converter transformer. With + 135v applied, the chopper alternates the + 135v return to develop the ac signal across the transformer. The secondaries are full wave rectified to produce the output dc voltage. The +5v is fed through the card cage to the front panel, lighting the POWER indicator.

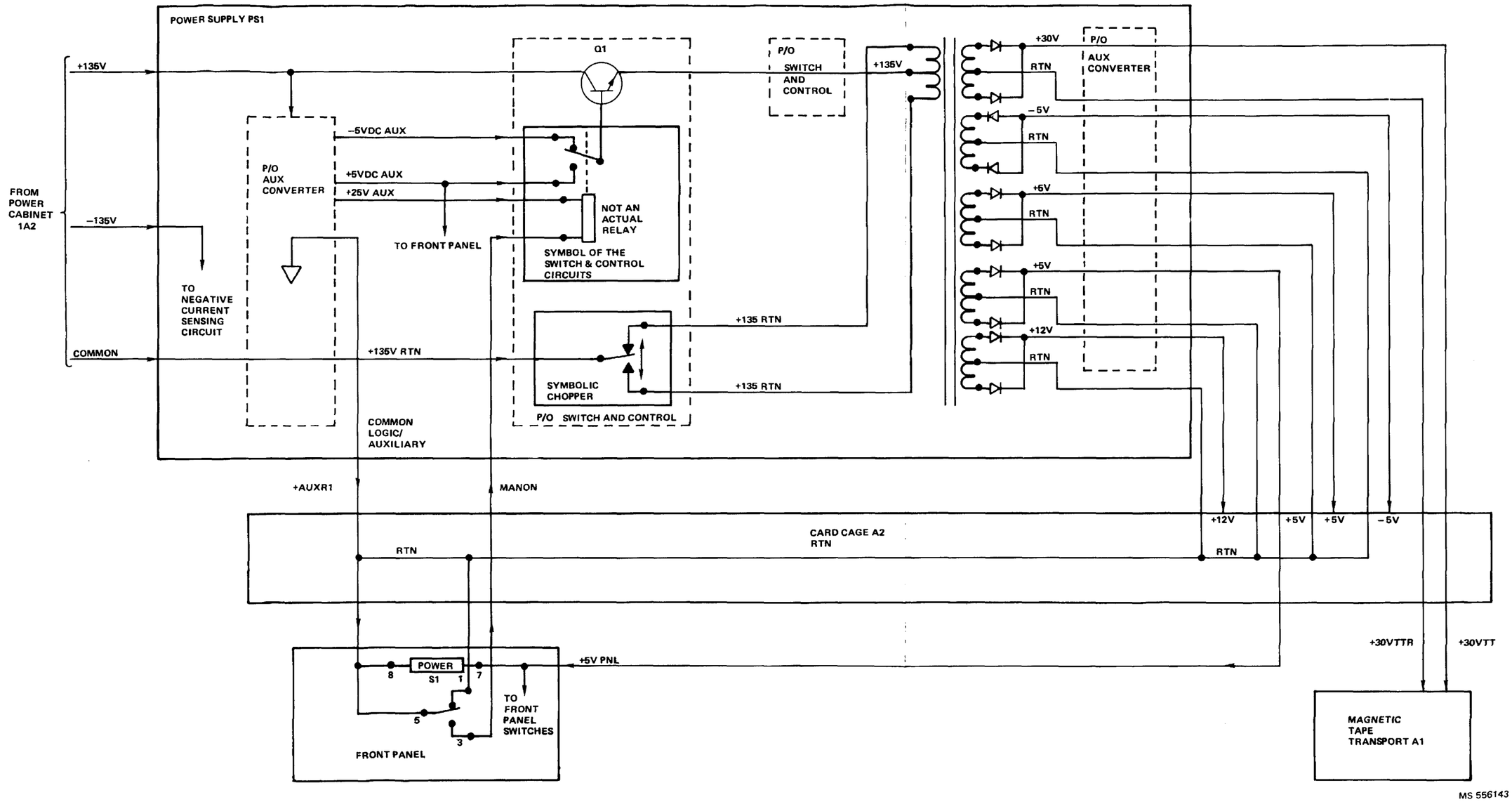


Figure 5-54. Power Distribution Block Diagram

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TEAR ALONG PERFORATED LINE

THE METRIC SYSTEM AND EQUIVALENTS

Linear Measure

1 centimeter = 10 millimeters = .39 inch
1 decimeter = 10 centimeters = 3.94 inches
1 meter = 10 decimeters = 39.37 inches
1 dekameter = 10 meters = 32.8 feet
1 hectometer = 10 dekameters = 328.08 feet
1 kilometer = 10 hectometers = 3.2808.8 feet

Weights

1 centigram = 10 milligrams = .15 grain
1 decigram = 10 centigrams = 1.54 grains
1 gram = 10 decigram = .035 ounce
1 dekagram = 10 grams = .35 ounce
1 hectogram = 10 dekagrams = 3.52 ounces
1 kilogram = 10 hectograms = 2.2 pounds
1 quintal = 100 kilograms = 220.46 pounds
1 metric ton = 10 quintals = 1.1 short tons

Cubic Measure

1 cu. centimeter = 1000 cu. millimeters = .06 cu. inch
1 cu. decimeter = 1000 cu. centimeters = 61.02 cu in.
1 cu. meter = 1000 cu. decimeters = 35.31 cu. feet

Square measure

1 sq. centimeter = 100 sq. millimeters = .155 sq. in.
1 sq. decimeter = 100 sq. centimeters = 15.5 inches
1 sq. meter (centare) = 100 sq. decimeters = 10.76 feet
1 sq. dekameter (are) = 100 sq. meters = 1.076.4 sq. ft.
1 sq. hectometer (hectare) = 100 sq. dekameters = 2.47 acres
1 sq. kilometer = 100 hectometers = .386 sq. miles

Liquid Measure

1 dekaliter = 10 liters = 2.64 gallons
1 hectoliter = 10 dekaliters = 26.42 gallons
1 kiloliter = 10 hectoliters = 264.18 gallons
1 liter = 10 deciliters = 33.81 fl. ounces
1 centiliter = 10 milliliters = .34 fl. ounce
1 deciliter = 10 centiliters = 3 38 fl. ounces
1 metric ton = 10 quintals = 1.1 short tons

Approximate Conversion Factors

To change	To	Multiply by
inches	centimeters	2.540
feet	meters	.305
yards	meters	.914
miles	kilometers	1.609
sq. inches	sq. centimeters	6.451
sq. feet	sq. meters	.093
sq. yards	sq. meters	.836
sq. miles	sq. kilometers	2.590
acres	sq. hectometers	.405
cubic feet	cubic meters	.028
cubic yards	cubic meters	.765
fluid ounces	milliliters	29.573
pints	liters	.472
quarts	liters	.946
gallons	liters	3.785
ounces	grams	28.349
pounds	kilograms	.454
short tons	metric tons	.907
pound inches	newton-meters	.11296

To change	To	Multiply by
ounce inches	newton-meters	.0070062
centimeters	inches	.394
meters	feet	3.280
meters	yards	1.094
kilometers	miles	.621
sq. centimeters	sq. inches	.155
sq. meters	sq. yards	10.764
sq. kilometers	sq. miles	1.196
sq. hectometers	acres	2.471
cubic meters	cubic feet	35.315
milliliters	fluid ounces	.034
liters	pints	2.113
liters	quarts	1.057
grams	ounces	.035
kilograms	pounds	2.205
metric tons	short tons	1.102
pound-feet	newton-meters	1.356

Temperature (Exact)

°F Fahrenheit temperature — 5/9 (after subtracting 32) — Celsius Temperature °C

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